

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**

(19) Japan Patent Office (JP)

(11) Japanese Patent Laid-Open Number: Hei 7-235255

(12) Publication of Unexamined Patent Applications (A)

(43) Laid-Open Date: Heisei 7-9-5 (September 5, 1995)

(51) Int. Cl.<sup>6</sup> Identification Code Office Reference Number F1

H 01 J 1/30 A

9/02 B

31/12 B

31/15 C

Request for Examination: No request to be done

Number of Claims: 30 OL (twenty-four pages in total)

(21) Application Number: Hei 6-141670

(22) Filed: Heisei 6-6-23 (June 23, 1994)

(31) Claim of Priority Number: Hei 5-335925

(32) Priority Date: Heisei 5-12-28 (December 28, 1993)

(33) Claim of Priority Country: Japan (JP)

(71) Applicant: 000001007

CANON INC.

30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo

(72) Inventor: Masato Yamanobe

CANON INC.

30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo

(72) Inventor: Ichiro Nomura

CANON INC.

30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo

(72) Inventor: Hidetoshi Suzuki

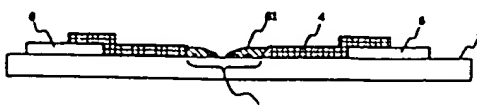
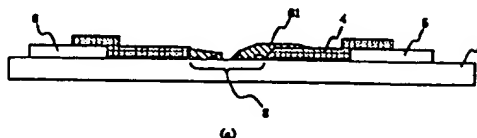
CANON INC.

30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo

(74) Agent: Attorney Giichi Marushima

to be continued to the last page

(54) [Title of the Invention] Electron Emission Device and Method of Manufacturing the Same, and Electron Source



Using Electron Emission Device and Image Formation Apparatus the Same  
(57) [Abstract] (Amended)

[Object] To provide a novel constitution of a surface conduction type electron emission device with a high efficiency and a method of manufacturing the same, and an electron source using the same and an image formation apparatus using the same.

[Constitution] An electron emission device having an electrically conductive film 4 including a high resistance portion, between electrodes 5 and 6 facing each other, the electron emission device having a sediment 61 containing carbon as a major constituent in the high resistance portion, a method of manufacturing the same, and an electron source using the same and an image formation apparatus using the same.

[Claims]

[Claim 1] An electron emission device which has an electrically conductive film including a high resistance portion, between electrodes facing each other, wherein a sediment containing carbon as a major constituent is provided in the high resistance portion.

[Claim 2] The electron emission device according to claim 1, wherein the sediment containing said carbon as a major constituent further exists in the vicinity of said high resistance portion.

[Claim 3] The electron emission device according to claim 2, wherein the sediment containing said carbon as a major constituent exists a region ranging from a part of said high resistance portion to said electrically conductive film.

[Claim 4] The electron emission device according to claim 3, wherein the sediment containing said carbon as a major constituent is unevenly distributed on a region ranging from a part of said high resistance portion to the electrically conductive film on one electrode side of said electrodes.

[Claim 5] The electron emission device according to claim 4, wherein the sediment containing said carbon as a major constituent is unevenly distributed on a region ranging from a part of said high resistance portion to the electrically conductive film on a high potential electrode of said electrodes.

[Claim 6] The electron emission device according to claim 1, wherein said electrically conductive film is formed of electrically conductive fine particles.

[Claim 7] The electron emission device according to claim 6, wherein said

electrically conductive fine particles are formed of a metal or a metal oxide.

[Claim 8] The electron emission device according to claim 6, wherein at least a part of said electrically conductive fine particles is covered with said sediment.

[Claim 9] The electron emission device according to claim 1, wherein said high resistance portion has electrically conductive particles.

[Claim 10] The electron emission device according to claim 9, wherein at least a part of said electrically conductive fine particles is covered with said sediment.

[Claim 11] The electron emission device according to claim 1, wherein the sediment containing said carbon as a major constituent covers at least a part of said electrodes.

[Claim 12] The electron emission device according to claim 1, wherein the sediment containing said carbon as a major constituent is graphite, amorphous carbon or mixture formed of graphite and amorphous carbon.

[Claim 13] The electron emission device according to claim 1, wherein an electron emission current shows a monotonous increasing characteristic for a voltage applied between said electrodes.

[Claim 14] An electron source which has an electron emission device, and emits electrons in response to an input signal, wherein said electron emission device is the electron emission device according to any one of claims 1 to 13.

[Claim 15] The electron source according to claim 14, wherein said electron emission device is provided in plural number, a plural number of lines of the electron emission devices, each of which has both ends connected by wiring, are provided, and modulation means for modulating electron rays emitted from the electron emission device is provided.

[Claim 16] The electron source according to claim 14, wherein said electron emission device is provided in plural number, the plurality of electron emission devices being disposed in parallel with each other so as to be connected to m X-direction wirings and n-direction wirings electrically insulated from each other.

[Claim 17] An image formation apparatus which has an electron source and an image formation member, and forms an image in response to an input signal, wherein said electron source has an electron emission device which

is the electron emission device according to any one of claims 1 to 13.

[Claim 18] The image formation apparatus according to claim 17, wherein said electron source has said electron emission device in plural number, a plural number of lines of the electron emission devices, each of which has both ends connected by wiring, are provided, and modulation means for modulating electron rays emitted from the electron emission device is provided.

[Claim 19] The image formation apparatus according to claim 17, wherein said electron source has said electron emission device in plural number, the plurality of electron emission devices being disposed in parallel with each other so as to be connected to m X-direction wirings and n-direction wirings electrically insulated from each other.

[Claim 20] The image formation apparatus according to claim 17, wherein an electron emission current of said electron source and a device current show a monotonous increasing characteristic for a voltage applied to the device.

[Claim 21] The image formation apparatus according to claim 17, wherein the image formation apparatus is kept to a vacuum so as to prevent a sediment containing said carbon as a major constituent from being newly deposited.

[Claim 22] A method of manufacturing an electron emission device which has an electrically conductive film including an electron emission portion between electrodes facing each other, comprising an activation step for activating the device.

[Claim 23] The method of manufacturing an electron emission device according to claim 22, wherein said activation step is a step for depositing a sediment containing carbon as a major constituent in said device.

[Claim 24] The method of manufacturing an electron emission device according to claim 23, wherein said activation step includes a step for applying a voltage to an electrically conductive film provided between the electrodes in vacuum.

[Claim 25] The method of manufacturing an electron emission device according to claim 24, wherein said voltage is applied in the form of pulses.

[Claim 26] The method of manufacturing an electron emission device according to claim 25, wherein said voltage is a voltage equal to a voltage

control type negative resistance characteristic region or more.

[Claim 27] The method of manufacturing an electron emission device according to claim 26, wherein said voltage is a driving voltage of an electron emission device.

[Claim 28] The method of manufacturing an electron emission device according to claim 22, the method further comprising a forming step.

[Claim 29] The method of manufacturing an electron emission device according to claim 28, wherein said forming step is a step for forming a high resistance portion in an electrically conductive film provided between the electrodes.

[Claim 30] The method of manufacturing an electron emission device according to claim 22, wherein said activation step is performed after said forming step.

[Detailed Description of the Invention]

[0001]

[Field of the Invention] The present invention relates to an electron source and an image formation apparatus such as a display device which is obtained by applying it, more particularly to a surface conduction type electron emission device having a novel constitution, an electron source using it, and an image formation apparatus such as a display device which is obtained by applying it.

[0002]

[Prior Arts] As an electron emission device, two kinds of devices including thermal electron sources and cold cathode electron sources have been heretofore known. The cold cathode electron sources include an electron emission type (hereinafter abbreviated to an FE type) electron emission device, a metal/insulating layer/metal type (hereinafter abbreviated to an MIN type) electron emission device and a surface conduction type electron emission device.

[0003] As an example of the FE type electron emission device, W. P. Dyke & W. W. Dolan, "Fieldemission", Advance in Electron Physics, 8, 89 (1956), C. A. Spindt, "PHYSICAL Properties of thin-film field emission cathodes with molybdenum cones", J. Appl. Phys., 47, 5248 (1976) and the like have been known.

[0004] As an example of the MIN type electron emission device, C. A. Mead,

"The tunnel-emission amplifier, J. Appl. Phys., 32,646 (1961) and the like have been known.

[0005] As an example of the surface conduction type electron emission device, M. I. Elinson, RadioEng. Electron Phs., 10, (1965) and the like have been known.

[0006] The surface conduction type electron emission device utilizes phenomenon in which electron emission occur in a thin film of a small area formed on a substrate by allowing a current to flow in parallel with a surface of the film. As the surface conduction type electron emission device, the one using a SnO<sub>2</sub> thin film by the foregoing Elinson, the one using Au thin film [G. Dittmer: "Thin Solid Films", 9, 317 (1972)], the one using In<sub>2</sub>O<sub>3</sub>/SnO<sub>2</sub> thin film [M. Hartwell and C. G. Fonstad: "IEEE Trans. ED Conf.", 519 (1975)], the one using a carbon thin film [Hisashi Araki and others: Vacuum, Vol. 26, No. 1, p 22 (1983)] have been reported.

[0007] A device structure by the foregoing M. Hartwell is shown in Fig. 18 as a typical device structure of these surface conduction type electron emission devices. In Fig. 18, reference numeral 1 denotes an insulating substrate. Reference numeral 2 denotes a thin film for forming an electron emission portion, which is formed of a metal oxide thin film formed to an H-shaped pattern by sputtering, and an electron emission portion 3 is formed by an electrifying treatment called a forming to be described later. Reference numeral 4 shall be referred to as a thin film including the electron emission portion. Note that L1 in the drawing is set to 0.5 to 1 mm and W is set to 0.1 mm.

[0008] In these surface conduction type electron emission devices, the electron emission portion 3 has generally been formed by the electrifying treatment called the forming as to the thin film 2 for forming an electron emission portion before performance of electron emissions. Specifically, the forming is performed in such manner that a DC voltage or a voltage which is very slowly boosted, for example, at a rate of about 1V/minute, is applied to both ends of the thin film 2 for forming an electron emission portion, to destroy, deform or transmute the thin film for forming an electron emission portion locally, and thus the electron emission portion 3 made to be an electrically high resistance state is formed. Note that in the electron emission portion 3, cracks occur in a part of the thin film 2 for forming an electron

emission portion and electron emissions are performed in the vicinity of the cracks. The thin film 2 for forming an electron emission portion which includes the electron emission portion formed by the forming shall be hereinafter referred to a thin film 4 including an electron emission portion. The surface conduction type electron emission device that has been subjected to the foregoing forming treatment emits electrons from its foregoing electron emission portion 3 by applying a voltage to the foregoing thin film 4 including an electron emission portion and allowing a current to flow there-through.

[0009] However, in these conventional surface conduction type electron emission devices, though there have been varieties of problems in putting them to practical use, the applicant of this application eagerly investigated various kinds of improvements as described later, and solved varieties of problems in putting them to practical use.

[0010] Since the foregoing surface conduction type electron emission devices have simple structures and can be manufactured easily, they have advantages that many can be arranged in a large area. Accordingly, various applications have been studied to make use of this feature. For example, charge beam sources, display devices and the like are enumerated.

[0011] As an example in which many surface conduction type electron emission devices are arranged, an electron source is enumerated in which the surface conduction type electron emission devices are arranged in parallel, and many lines obtained by connecting both ends of the respective devices by wiring are arranged. (e. g., Japanese Patent Laid-Open Sho 64-31332, Hei 1-283749, Hei 1-257552). Moreover, in image formation apparatuses such as display devices, particularly, though flat plate type display devices using liquid crystal have recently been popularized in place of CRTs, they are not self-luminous type, and they have troubles including a trouble with provision of a back light. Accordingly, development of self-luminous type display devices have been desired. Image formation apparatuses, which are display devices obtained by combining an electron source in which many surface conduction type electron emission devices are disposed and a phosphor emitting visible light by electrons emitted from the electron source, can be comparatively easily manufactured even when they have a large screen, and are a self-luminous type display device showing an excellent

display quality (e. g., USP 5066883).

[0012] Selection of a device emitting electrons to allow the phosphor to emit light, from the electron source constituted by many surface conduction type electron emission devices, is performed depending on a suitable driving signal to a wiring (called a row direction wiring) in which foregoing many surface conduction type electron emission devices are arranged in parallel, to a wiring (called a column direction wiring) in which they are arranged in a direction perpendicular to the row direction wiring, and to a control electrode (called a grid) arranged in a space between the electron source and the phosphor (e.g., Japanese Patent Laid-Open Hei 1-283749).

[0013]

[Subjects to be Solved by the Invention] However, behaviors of the surface conduction type electron emission device in vacuum, used for the foregoing electron source and the foregoing image formation apparatus, have not been almost known yet, and a stable and controlled electron emission characteristic and its increased efficiency have been desired.

[0014] Here, the efficiency means a current ratio of a current flowing when a voltage is applied to a pair of opposite device electrodes of the surface conduction type electron emission device (hereinafter referred to as a device current  $I_f$ ) to a current emitted in vacuum (hereinafter referred to as an emitted current  $I_e$ ).

[0015] Specifically, the device current should be as small as possible, and the emitted current should be as large as possible.

[0016] If the stable and controlled electron emission characteristic and the increased efficiency can be achieved, a high quality image formation apparatus displaying a bright image with a small current, for example, a flat television, can be realized in the image formation apparatus using the phosphor as the image formation member. Moreover, accompanied with the low current display, a lowering of cost of a driving circuit constituting the image formation apparatus can be expected. In view of the foregoing problems, the present invention provides a novel constitution of a high efficiency electron emission device which can be controlled stably and shows a device current as small as possible and an emitted current as large as possible, a method of manufacturing the same, an electron source using the same, and an image formation apparatus using the same.

[0017]

[Means for Solving the Subjects] An electron emission device to solve the foregoing subjects, which has an electrically conductive film including a high resistance portion, between electrodes facing each other, wherein a sediment containing carbon as a major constituent is provided in the high resistance portion. The electron emission device is preferably an electron emission device in which the sediment containing said carbon as a major constituent exists a region ranging from a part of the high resistance portion to the electrically conductive film. The electron emission device is more preferably an electron emission device in which the sediment containing the carbon as a major constituent is unevenly distributed on a region ranging from a part of the high resistance portion to the electrically conductive film on a high potential electrode of the electrodes.

[0018] A method of manufacturing the electron emission device which has an electrically conductive film including an electron emission portion between electrodes facing each other, comprising an activation step for activating the device. The activation step includes a step for depositing a sediment containing carbon as a major constituent in the device. The activation step preferably includes a step for applying a voltage in vacuum to an electrically conductive film provided between the electrodes.

[0019] The voltage is preferably applied in the form of pulses. The voltage is particularly preferably a driving voltage of the electron emission device.

[0020] Furthermore, the present invention is an electron source which has the above described electron emission device, and emits electrons in response to an input signal. The present invention is preferably an electron source in which the electron emission device is provided on a substrate, in which plural number of lines of the electron emission devices, each of which has both ends connected by wiring, are provided, the electron source having an arrangement style having modulation means or an arrangement style in which electron emission device is provided in plural number, the plurality of electron emission devices being disposed so that a pair of device electrodes are connected to m X-direction wirings and n Y-direction wirings electrically insulated from each other.

[0021] Moreover, the present invention is an image formation apparatus forming an image in response to an input signal, which has at least an im-

age formation member and the electron source of the present invention.

[0022] Preferable embodiments will be described below.

[0023] First, a basic constitution of a surface conduction type electron emission device according to the present invention will be described.

[0024] Figs. 1(a) and 1(b) are a plan view and a section view showing a constitution of a basic flat plate type surface conduction type electron emission device according to the present invention, respectively. The basic constitution of the device according to the present invention will be described using Fig. 1.

[0025] In Fig. 1, reference numeral 1 denotes a substrate; 5 and 6, a device electrode; 4, a thin film (electrically conductive film) including an electron emission portion; and 3, the electron emission portion.

[0026] As the substrate 1, enumerated are quartz glass, glass in which impurity contents such as Na and the like are reduced, blue plate glass, and a glass substrate obtained by laminating  $\text{SiO}_2$  formed by a sputtering method or the like on blue plate glass, ceramics such as alumina and the like.

[0027] Any material may be employed as materials of the device electrodes 5 and 6 facing each other as long as they have electrical conductivity, and enumerated are a printing conductor formed of metals such as Ni, Cr, Au, Mo, W, Pt, Ti, Al, Cu, and Ps or alloys of them, metals such as Pd, Ag, Au,  $\text{RuO}_2$  and Pd-Ag or metal oxides of them and glass, a transparent conductor formed of  $\text{In}_2\text{O}_3\text{-SnO}_2$ , and a semiconductor material such as polysilicon.

[0028] An inter-device electrode distance L1, a device electrode length W1 and a shape of the electrically conductive film 4 are properly designed in accordance with an application style of this device. For example, in a display device to be described later, a pixel size corresponding to a screen size is designed in a television, and in a high quality TV, above all, the pixel size is small, and a high definition is required. Therefore, in order to obtain a sufficient luminance under conditions that the size of the electron emission device is limited, designing is performed so as to obtain a sufficient emitted current.

[0029] The inter-device electrode distance L1 ranges from several hundred angstroms to several hundred micrometers, is set by a photolithography technology which is a base of a manufacturing method of the device electrode, that is, performance of an exposing machine and etching method, and

a voltage applied between the device electrodes and electric field intensity capable of emitting electrons. The inter-device electrode distance  $L_1$  should preferably range from several micrometers to several ten micrometers.

[0030] The length  $W_1$  of the device electrode and a film thickness  $d$  of the device electrodes 5 and 6 are properly designed based on a resistance value of the electrode, the connections of the foregoing X and Y wirings, and problems concerning arrangements of the electron sources arranged in plural number. The length  $W_1$  of the device electrode usually ranges from several micrometers to several hundred micrometers, and the film thickness  $d$  of the device electrodes 5 and 6 ranges from several hundred angstroms to several micrometers.

[0031] The thin film 4 including an electron emission portion provided between the device electrode 5 and the device electrode 6 facing each other, provided on the substrate 1, as well as provided on the device electrodes 5 and 6, includes the electron emission portion 3. However, the provision of the thin film 4 is not limited to the case shown in Fig. 1(b), and the thin film is not sometimes provided on the device electrodes 5 and 6. Specifically, the case where the thin film 2 for forming an electron emission portion and the device electrodes 5 and 6 facing each other are laminated on the insulating substrate 1 in this order holds true. Furthermore, all portions between the device electrodes 5 and 6 facing each other function sometimes as the electron emission portions depending on a way to manufacture the device. The film thickness of the thin film 4 including this electron emission portion should preferably range from several angstroms to several thousands angstroms, particularly from 10 angstroms to 500 angstroms. A step coverage to the device electrodes 5 and 6, a resistance value between the electron emission portion 3 and the device electrodes 5 and 6 and diameters of the electrically conductive fine particles of the electron emission portion 3 are properly set depending on electrifying treatment conditions described later. The resistance value shows a sheet resistance value of  $10^3$  to  $10^7$  ohm/ $\square$ .

[0032] When concrete examples of materials constituting the thin film (electrically conductive film) 4 including the electron emission portion are enumerated, metals such as Pd, Ru, Ag, Au, Ti, In, Cu, Cr, Fe, Zn, Sn, Ta, W

and Pb, oxides such as PdO, SnO<sub>2</sub>, In<sub>2</sub>O<sub>3</sub>, PbO and Sn<sub>2</sub>O<sub>3</sub>, borides such as HfB<sub>2</sub>, ZrB<sub>2</sub>, LaB<sub>6</sub>, CeB<sub>6</sub>, YB<sub>4</sub> and GdB<sub>4</sub>, carbides such as TiC, ZrC, HfC, TaC, SiC and WC, nitrides such as TiN, ZrN and HfN, semiconductors such as Si and Ge, and carbon, AgMg, NiCu, Pb and Sn are such concrete examples. They are fine particles.

[0033] The fine particle films described here are films in which a plurality of fine particles congregate. As a minute structure, there is not only a film in a state where the fine particles are individually dispersed but also a film in a state where the fine particles are adjacent to each other or superposed upon another, which includes an island-shape.

[0034] Diameters of the fine particles range from several angstroms to several thousands angstroms, preferably from 10 angstroms to 200 angstroms.

[0035] The electron emission portion 3 is, for example, a high resistance portion such as cracks, which is formed in a part of the electrically conductive film 4. The electron emission portion 3 has sometimes many fine particles of diameters preferably ranging from several angstroms to several hundreds angstroms, particularly preferably from 10 angstroms to 500 angstroms. The diameters of the fine particles depend on the film thickness of the thin film (electrically conductive film) 4 including the electron emission portion, and a manufacturing method such an electrifying treatment condition described later. The diameters thereof are appropriately set.

[0036] The foregoing electrically conductive fine particles are a substance identical to a part of elements of the materials constituting the thin film (electrically conductive film) 4 including the electron emission portion or to all of them.

[0037] Furthermore, carbon or carbon compound is deposited on a part of the electron emission portion 3 and the electrically conductive film 4 in the vicinity of the electron emission portion 3.

[0038] Next, a vertical type surface conduction type electron emission device that is the surface conduction type electron emission device having a different constitution according to the present invention will be described.

[0039] Fig. 12 is a schematic view showing a constitution of the basic vertical type surface conduction type electron emission device.

[0040] In Fig. 12, the constituent components denoted by the same reference numerals as those in Fig. 1 are identical to the constituent components in

Fig. 1. Reference numeral 21 denotes a step difference formation portion. A substrate 1, device electrodes 5 and 6, a thin film 4 including an electron emission portion, and an electron emission portion 3 are formed of the same materials as those in the foregoing flat plate type surface conduction type electron emission device. The step difference formation portion 21 is formed of an insulating material such as  $\text{SiO}_2$ , formed by a vacuum deposition method, a printing method, and a sputtering method. A film thickness of the step difference formation portion 21 corresponds to the inter-device electrode distance  $L$  of the foregoing flat plate type surface conduction type electron emission device, and ranges from several ten nanometers to several ten micrometers. The film thickness of the step difference formation portion 21 is set in accordance with a manufacturing method of the step difference formation portion, a voltage applied between the device electrodes, and an electric field intensity capable of emitting electrons, and preferably ranges from several ten nanometers to several micrometers. Since the thin film 4 including the electron emission portion is formed after formations of the electron electrodes 5 and 6 and the step difference formation portion 21, the thin film 4 is layered on the device electrodes 5 and 6. Note that the electron emission portion 3 is shown linearly in the step difference formation portion 21, depends on formation conditions and electrifying forming conditions, and a shape and a position thereof are not limited to this.

[0041] Various kinds of methods are conceived as a manufacturing method of the electron emission device having the electron emission portion 3. An example of the manufacturing method is shown in Fig. 2. Note that in Fig. 2, reference numeral 2 denotes a thin film for forming an electron emission portion (electrically conductive film), and, for example, a fine particle film is enumerated.

[0042] The manufacturing method will be sequentially described based on Fig. 1 and Fig. 2 below.

1) After the substrate 1 is sufficiently deterged by detergent, pure water or organic solvent, a device electrode material is deposited by a vacuum deposition method, a sputtering method and the like, followed by formation of the device electrodes 5 and 6 on the insulating substrate 1 by a photolithography technology (Fig. 2(a)).

2) Organic metal solvent is coated onto the insulating substrate on which the device electrodes 5 and 6 are formed, between the device electrodes 5 and 6 provided on the insulating substrate 1, and left as it is, whereby an organic metal thin film is formed. Note that the organic metal solvent is solution formed of organic compound containing as major elements metals such as the foregoing Pd, Ru, Ag, Au, Ti, In, Cu, Cr, Fe, Zn, Sn, Ta, W and Pb. Thereafter, the organic metal thin film undergoes a heating baking treatment, and is patterned by a lift-off and etching, thus forming the thin film 2 for forming the electron emission portion (Fig. 2(b)). Although description of the formation of the thin film 2 was made by a coating method of the organic metal solution, the formation thereof is not limited to this. The thin film 2 is sometimes formed by a vacuum evaporation method, a sputtering method, a chemical vapor deposition method, a dispersion coating method, a dipping method, a spinner method and the like.

3) Subsequently, when the electrifying treatment called a forming is performed by applying a pulse-shaped voltage from a power source (not shown) between the device electrodes 5 and 6 or by applying a boosted voltage therebetween, the electron emission portion 3 having a changed structure is formed in a portion of the thin film for forming the electron emission portion (electrically conductive film) 2 (Fig. 2(c)). By this electrifying treatment, the thin film for forming the electron emission portion (electrically conductive film) 2 is locally destroyed, deformed or changed its nature, and the portion (high resistance portion) where the structure is changed is called the electron emission portion 3.

[0043] Electrical treatments after the forming treatment are performed in a measurement evaluation apparatus shown in Fig. 3. The measurement evaluation apparatus will be described below.

[0044] Fig. 3 is a schematic constitution view of the measurement evaluation apparatus for measuring an electron emission characteristic of the device having the constitution shown in Fig. 1. In Fig. 3, reference numeral 1 denotes a substrate; 5 and 6, device electrodes; 4, a thin film including an electron emission portion; and 3, the electron emission portion. Moreover, reference numeral 31 denotes a power source for applying a device voltage  $V_f$  to the device; 30, a current meter for measuring the device current  $I_f$  flowing through the thin film 4 including the electron emission

portion between the device electrodes 5 and 6; 34, an anode electrode for capturing the emitted current  $I_e$  discharged from the electron emission portion of the device; 33, a high voltage source for applying a voltage to the anode electrode 34; and 32, a current meter for measuring the emitted current  $I_e$  discharged from the electron emission portion 3 of the device.

[0045] In measuring the foregoing device current  $I_f$  of the electron emission device, and the emitted current  $I_e$  thereof, the power source 31 and the current meter 30 are connected to the device electrodes 5 and 6, and the anode electrode 34 connecting the power source 33 and the current meter 32 is disposed above the electron emission portion. Moreover, the electron emission device and the anode electrode 34 are placed in a vacuum apparatus, and equipment such as an air exhaustion pump (not shown) and a vacuum gage (not shown), which are necessary for the vacuum apparatus, is provided in the vacuum apparatus, so that the measurement evaluation can be performed in a desired vacuum. Note that the air exhaustion pump is composed of an ordinary high vacuum apparatus system constituted by a turbo pump and a rotary pump or a high vacuum apparatus system without the use of oil such as magnetic levitation turbo pump and a dry pump, and an ultra high vacuum apparatus system constituted by an ion pump. Moreover, the whole of the vacuum apparatus and the power source substrate can be heated by a heater (not shown) to 200 °C.

[0046] Note that the voltage of the anode electrode was measured at a range from 1 kV to 10 kV, and the distance  $H$  from the anode electrode to the electron emission device was measured at a range from 2 mm to 8 mm.

[0047] The forming treatment is performed by applying pulses having a peak value that is a constant voltage, or by applying voltage pulses while increasing a pulse peak value. First, a voltage waveform when pulses having a pulse peak value that is a constant voltage is shown in Fig. 4(a).

[0048] In Fig. 4(a),  $T_1$  and  $T_2$  are a pulse width of a voltage waveform and a pulse interval thereof, and  $T_1$  is set to 1 microsecond to 10 milliseconds and  $T_2$  is set to 10 microseconds to 100 milliseconds. A peak value of a triangular wave (a peak voltage in the forming) is appropriately selected, and it is applied under vacuum atmosphere.

[0049] Next, a voltage waveform when voltage pulses are applied while increasing a pulse peak value is shown in Fig. 4(b).

[0050] In Fig. 4(b), T1 and T2 are a pulse width of a voltage waveform and a pulse interval thereof, and T1 is set to 1 microsecond to 10 milliseconds and T2 is set to 10 microseconds to 100 milliseconds. A peak value of a triangular wave (a peak voltage in the forming) is increased by about 0.1 V step, and is applied under vacuum atmosphere.

[0051] The forming treatment was finished when the device current was measured, the resistance value was obtained and it showed, for example, a value of 1 M ohm or more under a voltage of, for example, about 0.1 V that does not partially destroy and deform the thin film 2 for forming the electron emission portion during the pulse interval T2. The voltage at this time shall be called a forming voltage  $V_{\text{form}}$ .

[0052] When the electron emission portion described above is formed, the forming treatment is performed by applying the triangular pulse between the electrodes of the device. The waveform applied between the electrodes of the device is not limited to the triangular wave, a desired waveform such as a rectangular wave may be used, and its peak value, pulse width and pulse interval are not limited to the above values. Desired values are selected in accordance with resistance values of the electron emission device and the like so that the electron emission portion can be satisfactorily formed.

[0053] Moreover, since the forming voltage is uniquely determined depending on materials and constitutions of the device, the individual devices can obtain energy of the suitable forming more easily in the case where the voltage pulses are applied while increasing the pulse peak value as shown in Fig. 4(b), and a good electron emission characteristic can be preferably obtain.

4) Next, a treatment called an activation treatment is performed for the device that has been subjected to the forming treatment. The activation treatment is one in which pulses having a peak value that is a constant voltage are repeatedly applied similarly to the forming treatment at a vacuum ranging from about  $10^{-4}$  to  $10^{-5}$  Torr, and the device current  $I_f$  and the emitted current  $I_e$  significantly change by depositing carbon or carbon compound from organic substance existing in vacuum. While measuring the device current  $I_f$  and the emitted current  $I_e$ , for example, when the emitted current  $I_e$  saturates, the activation treatment is finished. An example of dependency of the device current  $I_f$  and the emitted current  $I_e$  on the acti-

vation treatment time is shown in Fig. 5.

[0054] The activation treatment depends on vacuum, a pulse voltage applied to the device, and the time dependency of the device current  $I_f$  and the emitted current  $I_e$  changes, and a formation state of a covering film (sediment) onto the thin film, which was deformed and changed in its nature, changes.

[0055] A case where a sufficiently high pulse of an activation treatment voltage compared to the forming voltage  $V_{form}$  is applied shall be a high resistance activation treatment. On the other hand, a case where a sufficiently low pulse of the activation treatment voltage compared to the forming voltage  $V_{form}$  is applied shall be a low resistance activation treatment. The activation treatment is classified depending on a level of a start voltage  $V_P$  showing a later described voltage control type negative resistance, to be correct, using the voltage  $V_P$  as a boundary.

[0056] Figs. 6(a) and 6(b) are schematic views showing an observation of a state change of the device in the case of the high resistance activation treatment and the low resistance activation treatment. Note that the above observation was performed by FESEM, TEM and the like.

[0057] Figs. 6(a) and 6(b) are section views of the device in the case where the high resistance activation treatment and the low resistance treatment were performed. Note that reference numeral 5 was used as a high potential side electrode, reference numeral 6 was used as a low potential side electrode, and an application of the voltage was performed. In Fig. 6(a) showing the case of the high resistance activation treatment, carbon or carbon compound 61 is mainly deposited on the electrically conductive film 4 on the high potential electrode 5 side rather than on a part of the portion (high resistance portion) 3 which is deformed like being fissured and changed in its nature by the forming. When the observation is performed with a higher magnification, the carbon or the carbon compound 61 is deposited also in the periphery of the fine particles. Moreover, the carbon or the carbon compound 61 is deposited also on the device electrodes sometimes depending on the distance between the device electrodes facing each other. A film thickness thereof should be preferably 500 angstroms or less, more preferably 300 angstroms or less.

[0058] Here, the carbon or the carbon compound includes graphite meaning

single crystalline and poly crystalline and amorphous carbon meaning compound formed of amorphous carbon and polycrystalline graphite as a result of TEM and Raman.

[0059] On the other hand, in Fig. 6(b) showing the case of the low resistance activation treatment, the carbon or the carbon compound 61 is deposited on a part of the portion 3 that has been deformed and changed in its nature by the forming. When the observation is performed with a higher magnification, the carbon or the carbon compound 61 is deposited also in the periphery of the fine particles.

[0060] Here, similarly to the above, the carbon or the carbon compound includes graphite meaning single crystalline and poly crystalline and amorphous carbon meaning compound formed of amorphous carbon and polycrystalline graphite as a result of TEM and Raman.

5) The electron emission device prepared as described above is preferably driven under vacuum atmosphere at vacuum higher than the vacuum at which the forming treatment and the activation treatment were performed. Moreover, the vacuum atmosphere at vacuum higher than the vacuum at which the forming treatment and the activation treatment were performed is one showing a vacuum of about  $10^{-6}$  Torr or more, more preferably one at which almost no carbon or carbon compound newly deposits in an ultra high vacuum system.

[0061] Accordingly, with such manner, it is possible to control additional deposit of the carbon or the carbon compound, and the device current  $I_f$  and the emitted current  $I_e$  are stabilized constantly.

[0062] Note that in the device in the case of the high resistance activation treatment and the low resistance activation treatment, a stability in an initial stage of driving differs, and more preferably the high resistance activation treatment is selected as the activation treatment.

[0063] A basic characteristic of the electron emission device according to the present invention, which was prepared by the device structure as described above and the manufacturing method, will be described using Fig.3 and Fig. 7.

[0064] A typical example of the relation among the emitted current  $I_e$ , the device current  $I_f$  and the device voltage  $V_f$  measured by the measurement evaluation apparatus shown in Fig. 3 is shown in Fig. 7. Since the emitted

current  $I_e$  is remarkably smaller than the device current  $I_f$ , Fig. 7 is illustrated in an optional measure. As is clear from Fig. 7, this electron emission device has three characteristics for the emitted current  $I_e$ .

[0065] First of all, when a device voltage equal to a certain voltage or more (referred to as a threshold voltage  $V_{th}$  in Fig. 7) is applied to this device, the emitted current  $I_e$  rapidly increases, and when a device voltage lower than the threshold voltage  $V_{th}$  is applied, the emitted current  $I_e$  is not almost detected. Specifically, this device is a nonlinear device having the clear threshold voltage  $V_{th}$  for the emitted current  $I_e$ .

[0066] Secondly, since the emitted current  $I_e$  depends on the device voltage  $V_f$ , the emitted current  $I_e$  can be controlled by the device voltage  $V_f$ .

[0067] Third, emitted charges captured in the anode electrode 34 depend on a time for which the device voltage  $V_f$  is applied. Specifically, a charge amount captured in the anode electrode 34 can be controlled by the time for which the device voltage  $V_f$  is applied.

[0068] On the other hand, the device current  $I_s$  sometimes shows a characteristic (solid lines in Fig. 7) in which the device current  $I_f$  monotonously increases for the device voltage  $V_f$  (called MI characteristic) and a voltage control type negative resistance (called VCNR characteristic) characteristic (broken lines in Fig. 7), and the characteristics of these device currents depend on the manufacturing methods thereof. In addition, a boundary voltage showing the VCNR characteristic is denoted as  $V_p$ .

[0069] Specifically, the VCNR characteristic of the device current  $I_f$  occurs when the forming is performed in an ordinary vacuum apparatus system and the VCNR characteristic was proved to largely change depending on a leaving time of the electron emission device in the vacuum apparatus until an electrical condition in the forming, a vacuum atmosphere condition in the vacuum apparatus system, a vacuum atmosphere condition of the vacuum apparatus system in measuring the electron emission device that has been already subjected to the forming, and an electrical measurement condition in measurement (for example, a sweep speed when the voltage applied to the device is swept from a low voltage to a high voltage to obtain a current-voltage characteristic of the electron emission device) are measured. In addition, at this time, the emitted current  $I_e$  shows a MI characteristic.

[0070] Since the electron emission device according to the present invention has the characteristic of the surface conduction type electron emission device as described above, that is, the monotonously increasing characteristic of the device current  $I_f$  and the emitted current  $I_e$  for the device application voltage, the electron emission device of the present invention can be expected to be applicable to many fields.

[0071] In the surface conduction type electron emission device constituted by previously dispersing the electrically conductive fine particles, the basic manufacturing method of the basic device structure of the present invention may be partially changed.

[0072] The basic constitution and the manufacturing method of the surface conduction type electron emission device were described as above, and according to a concept of the present invention, if the characteristic of the surface conduction type electron emission device has the foregoing three features, the device of the present invention is not limited to the above described constitution, and can be applied to a later described electron source and an image formation apparatus such as a display device.

[0073] Next, the electron source and the image formation apparatus of the present invention will be described.

[0074] The electron source and the image formation apparatus can be constituted by arranging the electron emission device of the present invention on a substrate in plural number.

[0075] As a method of an arrangement on the substrate, an arrangement style (hereinafter, referred to as a ladder type) is enumerated, in which many surface conduction type electron emission devices are arranged in parallel, many rows of the electron emission devices, both ends of which are connected by wiring, are arranged (called a row direction), and electrons are driven controllably by a control electrode (called a grid) disposed in a space above the electron source. An arrangement style is enumerated, in which  $n$  Y-direction wirings are placed on  $m$  X-direction wirings successively described interposing an interlayer insulating film, and the X-direction wirings and the Y-direction wirings are connected to a pair of device electrodes of the respective surface conduction type electron emission devices. This is hereinafter referred to as a simple matrix arrangement.

[0076] Next, this simple matrix will be described in detail.

[0077] According to the feature of the foregoing three basic characteristics of the surface conduction type electron emission device according to the present invention, emitted electrons from the surface conduction type electron emission device are controlled by a peak value of a pulse-shaped voltage and a width thereof applied between the opposite device electrodes in the threshold voltage or more. On the other hand, in the threshold voltage or less, the electrons are not almost emitted. According to this characteristic, even when many electron emission devices are arranged, if the above described pulse-shaped voltage is suitably applied to each device, the surface conduction type electron emission device is selected in accordance with an input signal, and its electron emission amount can be controlled.

[0078] A constitution of an electron source substrate constituted on the basis of this principle will be described using Fig. 8.

[0079] The  $m$  X-direction wirings 82 are composed of DX1, DX2,..., DX $m$ , and formed on the insulating substrate 1 by a vacuum evaporation method, a printing method, a sputtering method or the like. The X-direction wirings are formed of an electrically conductive metal or the like having a desired pattern, and a material, a film thickness and a width thereof are set so that approximately even voltages are applied to many surface conduction type electron emission device. The Y-direction wirings 83 are composed of  $n$  wiring including Dy1, DY2,..., DY $n$ , and formed by the vacuum evaporation method, the printing method, the sputtering method or the like, similarly to the X-direction wirings 82. The Y-direction wirings are formed of an electrically conductive metal or the like having a desired pattern, and a material, a film thickness and a width thereof are set so that approximately even voltages are applied to many surface conduction type electron emission device. Between the  $m$  X-direction wirings 82 and the  $n$  Y-direction wirings 83, an interlayer insulating layer (not shown) is formed, and the wirings 82 and 83 are electrically isolated, thus constituting the matrix wiring ( $m, n$ : positive integer).

[0080] The interlayer insulating layer (not shown) is SiO<sub>2</sub> or the like formed by the vacuum evaporation method, the printing method, the sputtering method or the like, and formed, in a desired shape, on the entire surface of the insulating substrate 1 on which the X-direction wirings 82 are formed or on a part of the insulating substrate 1. A film thickness, a material and a

manufacturing method of the interlayer insulating layer are appropriately set so that the interlayer insulating layer can resist a potential difference of a cross portion of the X-direction wirings 82 and the Y-direction wirings 83. The X-direction wirings 82 and the Y-direction wirings 83 are drawn out as an external terminal, respectively.

[0081] Moreover, similarly to the above, opposite electrodes (not shown) of the surface conduction type electron emission devices 84 are respectively connected to the  $m$  X-direction wirings 82 (DX1, DX2, ..., DX $m$ ) and the  $n$  Y-direction wirings 83 (DY1, DY2, ..., DY $n$ ) electrically by connection lines 85 formed of an electrically conductive metal or the like, formed by the vacuum evaporation method, the printing method, the sputtering method or the like.

[0082] Here, the electrically conductive metals forming the  $m$  X-direction wirings 82, the  $n$  Y-direction wirings 83, the connection lines 85 and the opposite device electrodes may be identical to each other in a part of constituent elements or all of them, and the electrically conductive metal is appropriately selected from a printing conductor formed of metals such as Ni, Cr, Au, Mo, W, Pt, Ti, Al, Cu, and Ps or alloys of them and metals such as Pd, Ag, Au, RuO<sub>2</sub> and Pd-Ag or metal oxides of them and glass, a transparent conductor formed of In<sub>2</sub>O<sub>3</sub>-SnO<sub>2</sub>, and a semiconductor material such as polysilicon. Moreover, the surface conduction type electron emission device may be formed on any of the insulating substrate 1 and the interlayer insulating layer (not shown).

[0083] Although the details are described later, scanning signal applying means (not shown) for applying a scan signal for scanning, in response to an input signal, the rows of the surface conduction type electron emission devices 84 arranged in the X-direction is electrically connected to the foregoing X-direction wirings 82. On the other hand, modulation signal generating means (not shown) for applying a modulating signal for modulating, in response to an input signal, the columns of the surface conduction type electron emission devices 84 arranged in the Y-direction is electrically connected to the foregoing Y-direction wirings 83.

[0084] Moreover, a driving voltage applied to each of the surface conduction type electron emission devices is supplied as a difference voltage between the scanning signal and the modulating signal, applied to the devices.

[0085] Next, the electron source using the electron source substrate pre-

pared in the above described manner and the image formation apparatus used for displays and the like will be described using Fig. 9 and Fig. 10. Fig. 9 is a basic constitutional view of the image formation apparatus, and Fig. 10 is a phosphor film.

[0086] In Fig. 9, reference numeral 1 denotes a substrate; 91, a rear plate fixing the substrate 1; 96, a face plate in which a phosphor film 94 and a metal back 95 are formed on an inner surface of a glass substrate 93; and 92, a supporting frame. Frit glass or the like is coated onto the rear plate 91, the supporting frame 92 and the face plate 96, and then baking at a temperature ranging from 400 °C to 500 °C for ten minutes or more in the air or nitrogen is performed for them. Thus, they are hermetically attached to each other, thus constituting an enveloper 98.

[0087] In Fig. 9, reference numeral 84 corresponds to the surface conduction type electron emission device shown in Fig. 1 or Fig. 12. Reference numerals 82 and 83 denote X-direction wirings and Y-direction wirings connected to a pair of device electrodes of the surface conduction type electron emission devices. Moreover, wirings connected to the device electrodes are sometimes called the device electrodes, when a material forming the device electrodes and a material forming the wiring are the same.

[0088] With reference to the enveloper 98, the enveloper 98 is composed of the face plate 96, the supporting frame 92 and the rear plate 91. However, since the rear plate 91 is provided to principally reinforce a strength of the substrate 1, if the substrate 1 itself has a sufficient strength, the separate rear plate 91 is unnecessary, and the enveloper 98 may be constituted by the face plate 96, the supporting frame 92 and the substrate 1 by attaching the supporting frame 92 directly to the substrate 1 hermetically.

[0089] Fig. 10 is a phosphor film. Although the phosphor film 94 is formed of only phosphor in the case of monochrome, the phosphor film 94 is composed of a black conductor material 101 and a phosphor 102, called a black stripe or a black matrix depending on an arrangement of the phosphor, in the case of a color phosphor film. The object of the provision of the black stripe and the black matrix is to make color mixing inconspicuous by blackening painting separation portion between the phosphors 102 of three primary color phosphors necessary for a color display, and to suppress a reduction in contrast due to external light reflection in the phosphor film 94.

As a material of the black stripe, in addition to a material containing graphite as a major constituent generally used, any material may be used as long as it shows an electrical conductivity and less light transmittance and reflectance.

[0090] As a method to coat the phosphor onto the glass substrate 93, a sedimentation method and a printing method are used without depending on monochrome and color.

[0091] Moreover, a metal back 95 is usually provided on an inner surface of the phosphor film 94. The object of the provision of the metal back is to increase luminance by mirror reflecting light among light generated by the phosphor to the face plate 96 side, the light travelling to the inner surface, and to allow the metal back 95 to act as an electrode for applying an electron beam acceleration voltage, and to protect the phosphor from damages due to collisions of negative ions generated in the enveloper. The metal back can be made by performing a smoothing treatment (usually called a forming) for the inner surface of the phosphor film after preparation of the phosphor film, and by depositing Al by the vacuum evaporation or the like.

[0092] A transparent electrode (not shown) may be provided in the face plate 96 to further increase electrical conductivity of the phosphor film 94.

[0093] When the foregoing hermetic attachment is performed, since each color phosphor and the electron emission device must correspond to each other in the case of color, sufficient positioning must be conducted.

[0094] The enveloper 98 is made to be vacuum of about  $10^{-6}$  Torr via an air exhaustion pipe (not shown), and the enveloper 98 is sealed.

[0095] The electron source substrate may have a structure that the device of Fig. 1 or Fig. 12 in which the electron emission portion is formed as described above is arranged and wired on the substrate as described above. The electron source substrate is more preferably prepared in such manner that devices before the formation of the electron emission portion, for example, the devices in a state of Fig. 2(b), are arranged and wired on the substrate, the assembled body is disposed within the enveloper 98 shown in Fig. 9, followed by making the enveloper at vacuum of about  $10^{-6}$  Torr by an ordinary vacuum apparatus system using a pump system such as a rotary pump and a turbo pump via an air exhaustion pipe (not shown), a voltage is applied between the device electrodes 5 and 6 (Fig. 2(b)) through the envel-

oper external terminals Dox1 to Doxm and Doy1 to Doyn, the foregoing forming is performed, and the foregoing activation treatment is performed while keeping the inside of the envelope 10 at a vacuum of about  $10^{-6}$  Torr, thus forming the electron emission portion 3.

[0096] After the formation of the electron source substrate in the above described manner, the vacuum apparatus system is changed to an ultra high vacuum apparatus system using a pump system such as an ion pump, while performing baking at a temperature ranging from 80 to 150 degrees for a time ranging from 3 to 15 hours. The switching to the ultra high vacuum apparatus system and the baking are performed to satisfy the monotonously increasing characteristic (MI characteristic) of the device current  $I_f$  and the emitted current  $I_e$  of the foregoing surface conduction type electron emission device. The method and conditions of the formation of the electron source substrate are not limited to this. Moreover, to maintain the vacuum after sealing the envelope 98, a gettering treatment is sometimes performed. This gettering treatment is one performed in such manner that immediately before sealing the envelope 98 or after sealing the envelope 98, a getter disposed at a predetermined position (not shown) of the envelope 98 is heated, and thus an evaporation film is formed. The getter usually contains Ba as a major constituent, and serves to maintain a vacuum of, for example, about  $1 \times 10^{-5}$  to  $1 \times 10^{-7}$  Torr by an absorption action of the evaporation film.

[0097] In the image display device of the present invention completed in the above described manner, a voltage is applied to each electron emission device through the container external terminals Dox1 to Doxm, and Doy1 to Doyn, and thus electrons are emitted therefrom. A voltage of several kV or more is applied to the metal back 95 and a transparent electrode (not shown), and thus electron beam is accelerated so as to collide against the phosphor film 94, and the phosphor film 94 is excited and allowed to emit light, thus displaying an image.

[0098] The constitution described above is schematic constitution necessary for preparing the preferable image formation apparatus used for a display. The detail portions such as a material of each member are not limited to the foregoing contents, and appropriately selected so as to fit use of the image device.

[0099]

[Embodiments] The present invention will be described below in detail while citing embodiments.

[0100] (Embodiment 1) A constitution of a basic surface conduction type electron emission device according to the present invention is the same as the plan view and the section view of Figs. 1(a) and 1(b).

[0101] Four devices having the same shape are formed on a substrate 1 as shown in Fig. 11. Note that in Fig. 11, the same reference numerals as those of Fig. 1 represent the same constituent components.

[0102] A manufacturing method of the surface conduction type electron emission device according to the present invention is principally the same as those of Fig. 2. Using Fig. 1 and Fig. 2, a basic constitution of the device according to the present invention and a manufacturing method thereof will be described below.

[0103] In Fig. 1, reference numeral 1 denotes a substrate; 5 and 6, a device electrode; 4, a thin film including an electron emission portion; and 3, the electron emission portion.

[0104] Descriptions of the manufacturing method will be sequentially described with reference to Fig. 1 and Fig. 2 below.

[0105] Step-a: On the substrate 1 in which a silicon oxide film of a thickness of 0.5 microns is formed on a cleaned blue plate glass by a sputtering method, a pattern serving as a device electrode 5 and an inter-device electrode gap G is formed by photoresist (RD-2000N-41 manufactured by Hitachi Chemical Co. Ltd.), and Ti of a thickness of 50 Å and Ni of a thickness of 1000 Å are sequentially deposited by an evaporation vacuum method. The photoresist pattern is dissolved by organic solvent, and the Ni/Ti deposited film is lifted off. The inter-device electrode gap G is set to 3 microns, and thus the device electrodes 5 and 6 having the width W1 of 300 microns were formed (Fig. 2(a)).

[0106] Step-b: By a vacuum evaporation method, a Cr film 121 of a thickness of 1000 Å is deposited and patterned by the inter-device electrode gap G and a mask having an opening in the vicinity of inter-device electrode gap G, and organic Pd (ccp 4230 manufactured by OKUNO CHEMICAL INDUSTRIES CO., LTD.) is coated onto the Cr film 121 while rotating by a spinner. A thermal baking treatment was performed at a temperature

300 °C for 10 minutes. A film thickness of the thin film 2 for forming the electron emission portion formed in the above described manner, which is formed of fine particles containing Pd as a major constituent, was 100 angstroms, and a sheet resistance value thereof was  $2 \times 10^4 \Omega/\square$ . The fine particle film described here is a film in which the plurality of fine particles are aggregated as described above, and in terms of its minute structure, the thin film 2 is a film in which fine particles are dispersively disposed individually, a film in which the fine particles are adjacent to each other, or a film in which the fine particles are superposed (including an island shape). Diameters of the fine particles are diameters of fine particles of shapes that can be recognized in said state.

[0107] Step-c: The Cr film and the thin film 2 for forming the electron emission portion after baking were etched by acid etchant, thus forming a desired pattern. The device electrodes 5 and 6, the thin film 2 for forming the electron emission portion and the like were formed on the substrate 1 by the above described steps (Fig. 2 (b)).

[0108] Step-d: Next, the assembly was set in the measurement evaluation apparatus of Fig. 3, and air is discharged therefrom by a vacuum pump. After a vacuum of  $2 \times 10^{-5}$  Torr was obtained, an electrifying treatment (forming treatment) was performed, while applying a voltage between the device electrodes 5 and 6 of the four devices by the power source 31 for applying the device voltage  $V_f$  to the devices. The voltage waveform of the forming treatment is shown in Fig. 4(b).

[0109] In Fig. 4(b), T1 and T2 represent the pulse width of the voltage waveform and the pulse interval thereof, and in this embodiment T1 is set to 1 millisecond and T2 is set to 10 milliseconds. A peak value (peak voltage in the forming treatment) of the rectangular wave is boosted in 0.1 V step, and the forming treatment was performed. Moreover, during the forming treatment, a resistance measurement pulse with a volt of 0.1 V was inserted in T2, and the resistance was measured. The forming treatment was terminated when the measurement value in the resistance measurement pulse becomes equal to about 1 M ohm or more, and, at the same time, an application of the voltage to the device was finished. The forming voltages  $V_{form}$  of the respective devices were 5.1 V, 5.0 V, 5.0 V, 5.1 V and 5.15 V.

[0110] Step-e: Subsequently, for the four devices that have been subjected to

the forming treatment, two sets of two devices were subjected to the activation treatment, respectively, with rectangular waves having peak values of 4 V and 14 V, shown in Fig. 4(b). The device sample that has been subjected the activation treatment with 4 V, that is, the low resistance activation treatment, shall be called a device A, and the device sample that has been subjected the activation treatment with 14 V, that is, the high resistance activation treatment, shall be called a device B.

[0111] During the activation treatment, as described above, the pulse voltage was applied between the device electrodes in the measurement evaluation apparatus of Fig. 3 while measuring the device current  $I_f$  and the emitted current  $I_e$ . At this time, a vacuum in the measurement evaluation apparatus of Fig. 3 was  $1.5 \times 10^{-5}$  Torr. The activation treatment was terminated after the elapse about 30 minutes.

[0112] In the above described manner, the electron emission portion 3 was formed, and thus the electron emission device was prepared

[0113] To grasp the characteristic and form of the surface conduction type electron emission device prepared according to the above described steps, as to each one of the above described devices A and B, the electron emission characteristic of each one was measured using the foregoing measurement evaluation apparatus of Fig. 3. Remaining each one thereof is observed with an electron microscope.

[0114] Note that the distance between the anode electrode and the electron emission device was set to 4 mm, the voltage of the anode electrode was set to 1 kV, and the vacuum in the vacuum apparatus during the electron emission characteristic measurement was set to  $1 \times 10^{-6}$  Torr. As to both of the devices A and B, the device voltage of 14 V was applied between the electrodes 5 and 6, and the device current  $I_f$  and the emitted current  $I_e$  were measured at this time. In the device A, the device current  $I_f$  of about 10 mA flowed immediately after starting the measurement, and gradually decreased. Accompanied with this, the emitted current  $I_e$  was observed. On the other hand, in the device B, the stable device current  $I_f$  and emitted current  $I_e$  were observed from an early stage of the measurement, and, when the device voltage was 14 V, the device current  $I_f$  was 2.0 mA and the emitted current  $I_e$  was 1.0  $\mu$ A. The electron emission efficiency  $\eta = I_e/I_f \times 100$  (%) was 0.05 %. From the above, the device A showed a very large and

unstable device current  $I_f$  in the early stage of the measurement. On the other hand, the device B is proved to be an electron emission device which is stable and shows a good efficiency  $\eta$  from the early stage of the measurement.

[0115] Moreover, with the device B, the vacuum was restored to  $5 \times 10^{-5}$ , and when the device current  $I_f$  and the emitted current  $I_e$  were measured while sweeping the voltage for the device with a triangular wave of about 0.005 Hz, the characteristics shown by the broken lines in Fig. 7 were showed. As shown in Fig. 7, the device current  $I_f$  monotonously increases up to the vicinity of about 5 V, and then shows the voltage control type negative resistance. At this time, a voltage (called  $V_p$ ) at which the device current  $I_f$  shows the maximum value is 5 V. Furthermore, for a voltage of 10 V or more, the device current  $I_f$  was about 1 mA equal to one fifth to sixth of the maximum device current  $I_f$ . The forms of the devices A and B observed by the electron microscope are the same as those shown in Figs. 6(a) and 6(b). From (B) of Fig. 6, in the device A, it is proved that many covering films (sediment) 61 are formed on a part of the degenerated portion 3 of the thin film (electrically conductive film) 4 between the device electrodes. On the other hand, in the device B, from Fig. 6(a), depending on the application direction of the voltage to the device during the activation treatment, the covering film (sediment) was formed mainly on a region from a part of the degenerated portion 3 to the electrically conductive film 4 on the high potential electrode 5 side. Moreover, when the observation was made by a high magnification FESEM (abbreviation of a secondary electron microscope), this covering film seemed to be formed around the metal fine particles and between the fine particles.

[0116] Note that when the observation was performed by a TEM (transmission electron microscope) Raman, a carbon covering film formed of graphite and amorphous carbon was observed.

[0117] Based on these observation, it is considered that since the device A was activated at a voltage of  $V_p$  or less showing the foregoing voltage control type negative resistance, much carbon was formed from the device B in a part of the degenerated portion of the thin film generated by the forming treatment, a very large device current flowed, the carbon covering film formed between the high and low potential sides of the thin film degenerat-

ed portion acts as a current path with the measurement voltage, the device current several times as much as that of the device B flowed, and the device current changed from the initial stage of the driving.

[0118] On the other hand, in the device B for which the high resistance activation treatment was performed, the device B was activated at a voltage of  $V_p$  or more showing the foregoing voltage control type negative resistance. Though the carbon covering film was formed on a part of the degenerated portion similarly to the device A, it is considered that there are more electrically cut portions in a part of the carbon covering film than in the device A. Accordingly, it is considered that a stable current was generated from the initial stage of the driving.

[0119] As described above, by the high resistance activation treatment, the device current  $I_f$  and the emitted current  $I_e$  were stabilized and the high efficiency electron emission device was prepared.

[0120] (Embodiment 2) This embodiment is an example of an image formation apparatus in which many surface conduction type electron emission devices are arranged in a simple matrix style.

[0121] A plan view of a part of an electron source is shown in Fig. 13. Furthermore, a A-A' section view in Fig. 13 is shown in Fig. 14. Note that constituent components denoted by the same reference numerals as those in Figs. 13, 14, 15 and 16 represent the same constituent components. Here, reference numerals 1 denotes a substrate; 82, X-direction wirings (referred to as lower wirings) corresponding to  $D_{xm}$  of Fig. 8; 83, Y-direction wirings (referred to as upper wirings) corresponding to  $D_{yn}$  of Fig. 8; 4, a thin film including a electron emission portion; 5 and 6, a device electrode; 141, an interlayer insulating layer; and 142, a contact hole for electrically connecting the device electrode 5 and the lower wirings 82.

[0122] Next, a manufacturing method will be concretely described by Fig. 15 and Fig. 16 in the order of steps.

[0123] Step-a: On the substrate 1 in which a silicon oxide film of a thickness of 0.5 microns is formed on a cleaned blue plate glass by a sputtering method, Cr of a thickness of 50 angstroms and Au of a thickness of 6000 angstroms are sequentially layered by a vacuum evaporation method, and then photoresist (AZ1370 manufactured by Hoechst Japan Limited) was coated thereonto while rotating by a spinner. The photoresist is baked, and

thereafter, the photomask image is exposed and developed, and a resist pattern of the lower wirings 82 is formed. The Au/Cr deposit film having a desired shape is wet-etched, and the lower wirings 82 are formed (Fig. 15(a)).

[0124] Step-b: Next, the interlayer insulating layer 141 formed of a silicon oxide film having a thickness of 1.0 micron is deposited by a RF sputtering method (Fig. 15(b)).

[0125] Step-c: A photoresist pattern for forming the contact hole 142 in the silicon oxide film that has been deposited in the foregoing step is formed, and the interlayer insulating layer 141 is etched using the pattern as a mask, thus forming the contact hole 142. The etching was performed according to a RIE (Reactive Ion Etching) method using  $\text{CF}_4$  gas and  $\text{H}_2$  gas (Fig. 15(c)).

[0126] Step-d: Thereafter, a pattern serving as a device electrode 5 and an inter-device electrode gap G is formed by photoresist (RD-2000N-41 manufactured by Hitachi Chemical Co. Ltd.), and Ti of a thickness of 50 angstroms and Ni of a thickness of 1000 angstroms are sequentially deposited by an evaporation vacuum method. The photoresist pattern is dissolved by organic solvent, and the Ni/Ti deposited film is lifted off. The inter-device electrode gap G is set to 3 microns, and the device electrodes 5 and 6 having the width W1 of 300 microns were formed (Fig. 15(d)).

[0127] Step-e: After a photoresist pattern of the upper wiring 83 is formed on the device electrodes 5 and 6, Ti having a thickness of 50 angstroms and Au having a thickness of 5000 angstroms are sequentially deposited by a vacuum evaporation, and an unnecessary portion is removed by lifting-off, thus forming the upper wiring 84 having a desired shape (Fig. 16(e)).

[0128] Step-f: A Cr film 151 having a thickness of 1000 angstroms is deposited by the vacuum evaporation, and patterned. Organic Pd (ccp 4230 manufactured by OKUNO CHEMICAL INDUSTRIES CO., LTD.) is coated thereonto by a spinner. A thermal baking treatment was performed at a temperature 300 °C for 10 minutes. A film thickness of the thin film 2 for forming the electron emission portion formed in the above described manner, which is formed of fine particles containing Pd as a major constituent, was 85 angstroms, and a sheet resistance value thereof was  $3.9 \times 10^4 \Omega/\square$ . The fine particle film described here is a film in which the plurality of fine

particles are aggregated as described above, and in terms of its minute structure, the thin film 2 is a film in which fine particles are dispersively disposed individually, a film in which the fine particles are adjacent to each other, or a film in which the fine particles are superposed (including an island shape). Diameters of the fine particles are diameters of fine particles of shapes that can be recognized in said state (Fig. 16(f)).

[0129] Step-g: The Cr film 151 and the thin film 2 for forming the electron emission portion after baking were etched by acid etchant, thus forming a desired pattern (Fig. 16(g)).

[0130] Step-h: A pattern so as to coat resist on a region other than the contact hole 142 was formed, and Ti having a thickness of 50 angstroms and Au having a thickness of 5000 angstroms were sequentially deposited by a vacuum evaporation. By removing an unnecessary portion by lifting-off, the contact hole 142 was buried (Fig. 16(h)).

[0131] By the foregoing steps, the lower wirings 82, the interlayer insulating layer 141, the upper wirings 83, the device electrodes 5 and 6 and the thin film 2 for forming the electron emission portion were formed on the insulating substrate 1.

[0132] Next, using the electron source substrate prepared in the above described manner, an example constituting the electron source and the display device will be described using Fig. 9 and Fig. 10.

[0133] After the substrate 1 on which the device was prepared in the above described manner was fixed onto the rear plate 91, the face plate 96, which is constituted by forming the phosphor film 94 and the metal back 95 on an inner surface of the glass substrate 93, was disposed above the substrate 1 with a space of 5 mm via the supporting frame 92, and frit glass was coated onto a junction portion of the face plate 96, the supporting frame 92 and the rear plate 91. Baking was performed in the air or in nitrogen atmosphere for 400 °C to 500 °C for 10 minutes or more, thus sealing the junction portion. Moreover, fixing of the substrate 1 to the rear plate 91 was performed by the frit glass.

[0134] In this embodiment, reference numeral 84 of Fig. 9 is the electron emission device before the formation of the electron emission portion, which corresponds to for example, Fig. 2(b), and reference numerals 82 and 83 are device electrodes in the X and Y-directions, respectively.

[0135] The phosphor film 94 is formed of only phosphor in the case of monochrome, and in this embodiment adopted a stripe shape (Fig. 10(a)). A black stripe was previously formed, and the phosphors having respective colors were coated onto gap portions thereof, thus forming the phosphor film 94. A material containing graphite as a major constituent, which has been usually used widely, was used as the material of the black stripe. A method for coating the phosphor onto the glass substrate 93 used a slurry method.

[0136] Moreover, the metal back 95 is usually provided on the inner surface of the phosphor film 94. The metal back was prepared in such manner that after the formation of the phosphor film, a smoothing treatment for the inner surface of the phosphor film, which is usually called a filming, was performed, and then Al was deposited in vacuum.

[0137] In the face plate 96, a transparent electrode (not shown) may be provided in the outer surface of the phosphor film 94 to further increase electrical conductivity of the phosphor film 94. In this embodiment, the transparent electrode was omitted because a sufficient electrical conductivity can be obtained only by the metal back.

[0138] When the foregoing sealing was performed, since the phosphors of each color and the electron emission devices had to correspond to each other in the case of color, positioning was performed sufficiently.

[0139] The atmosphere in the glass container completed in the above described manner was exhausted by a vacuum pump through an air exhaustion pipe (not shown), and after a sufficient vacuum was obtained, a voltage was applied between the electrodes 5 and 6 of the electron emission device 74 through the container external terminals Dxo1 to Dxom and Doy1 to Doyn, and the thin film 2 for forming the electron emission portion was subjected to the forming treatment. The voltage waveforms of the forming treatment is the same as that of Fig. 4(b).

[0140] In this embodiment, T1 was set to 1 millisecond, and T2 was set to 10 milliseconds, and the forming treatment was performed at a vacuum of about  $1 \times 10^{-5}$  Torr.

[0141] The electron emission portion 3 prepared in such manner got a state where fine particles containing palladium elements are dispersively arranged, and average diameters of the fine particles were 30 angstroms.

[0142] Next, the high resistance activation treatment was performed with the same rectangular wave as that of the forming and a peak value of 14 V at a vacuum of  $2 \times 10^{-5}$  Torr, while measuring the device current  $I_f$  and the emitted current  $I_e$ .

[0143] The forming treatment and the activation treatment were performed, and the electron emission portion 3 was formed, thus forming the electron emission device 84.

[0144] Next, an air exhaustion was performed to about a vacuum of  $10^{-6}$  Torr, and an air exhaustion pipe (not shown) was heated by a gas burner, thus sealing the envelope.

[0145] Finally, to maintain the vacuum after sealing, a getter treatment was performed by a high frequency heating method.

[0146] In the image display device of the present invention completed in the above described manner, a scanning signal and a modulating signal were applied to each electron emission device through the container external terminals Dx1 to Dxm, and Dy1 to Dyn by signal generating means (not shown), and thus electrons were emitted therefrom. A voltage of 5 kV or more was applied to the metal back 95 through the high voltage terminal Hv, thus accelerating electron beam so as to collide against the phosphor film 99, and the phosphor film 99 was excited and allowed to emit light, thus displaying an image. Moreover, both of the device current  $I_f$  and the emitted current  $I_e$  showed the solid lines of Fig. 7, and were stable from the initial stage of driving. In addition, it was the emitted current that was capable of coping with luminance of 100 fL to 150 fL required for televisions.

[0147] (Embodiment 3) Fig. 17 is a view for showing an example of a display device which is constituted so as to be capable of displaying image information on a display panel using the surface conduction type electron emission device described above, which is supplied from various kinds of image information sources such as TV broadcasts. In Fig. 17, reference numeral 17100 denotes a display panel; 17101, a driving circuit of the display panel; 17102, a display controller; 17103, a multiplexer; 17104, a decoder; 17105, an I/O interface circuit; 17106, a CPU; 17107, an image generating circuit; 17108, 17109 and 17110, an image memory interface circuit; 17111, an image input interface circuit; 17112 and 17113, a TV signal receiving circuit; and 17114, an input section. Note that when signals including both of

video information and voice information as television signals are received, the present display device performs reproduction of voice as well as displaying video information, however, descriptions for a speaker and circuit concerning receiving, separating, reproducing and storing voice information having no direct relations with the features of the present invention are omitted.

[0148] Functions of each portion will be described along a flow of an image signal below.

[0149] First, the TV signal receiving circuit 17113 is a circuit for receiving a TV image signal transmitted by use of a radio transmission system such as radio wave and spatial optical communication. A method of the TV signals received is not especially limited. Various kinds of forms such as a NTSC method, a PAL method and SECAM method may be adopted. The TV signals composed of more scanning lines than these, for example, so called a high quality TV including a MUSE method, are signal sources suitable for making use of the foregoing display panel suitable for a large area and a large number of pixels. The TV signals received by the TV signal receiving circuit 17113 are output to the decoder 17104.

[0150] Moreover, the TV signal receiving circuit 17112 is a circuit for receiving TV image signals transmitted by use of a cable transmission system such as a coaxial cable and an optical fiber. Similarly to the foregoing TV signal receiving circuit 17113, a method of the TV signals received is not especially limited, and the TV signals received by this circuit are output to the decoder 17104.

[0151] Moreover, the image input interface circuit 17111 is a circuit for fetching in image signals supplied from an image input device such as a TV camera and an image reading-out scanner, and the fetched image signals are output to the decoder 17104.

[0152] The image memory interface circuit 17110 is a circuit for fetching in image signals stored in a video tape recorder (hereinafter abbreviated to as VTR), and the fetched image signals are output to the decoder 17104.

[0153] Furthermore, the image memory interface circuit 17109 is a circuit for fetching in image signals stored in a video disc, and the fetched image signals are output to the decoder 17104.

[0154] The image memory interface circuit 17108 is a circuit for fetching in

image signals from a device such as a still image disc, which stores still image data, and the fetched still image data is input to the decoder 17104. Furthermore, the I/O interface circuit 17105 is a circuit for connecting a display device to an external computer, a computer network, and an output device such as a printer. The I/O interface circuit 17104 performs, as a matter of course, input/output for image data, and character/graphical information, and can, in some cases, perform input/output for a control signal and numerical data between a CPU 17106 which the present display device provides and the outside.

[0155] The image generating circuit 17107 is a circuit for generating display image data based on image data and character/graphical information input from the outside via the foregoing I/O interface circuit 17105 and based on image data and character/graphical information output from the CPU 17106. Within this circuit, incorporated are circuits necessary for generating images, such as a rewritable memory for storing, for example, image data and characters/graphical information, a read-only memory in which an image pattern corresponding to a character code is stored, and a processor for performing an image processing.

[0156] The display image data generated by this circuit is output to the decoder 17104, and, in some cases, can be output to an external computer network and a printer via the foregoing I/O interface circuit 17105.

[0157] The CPU 17106 performs mainly an operation control of the present display device and operations concerning generation, selection and editing of the display image.

[0158] The CPU 17106 outputs, for example, a control signal to the multiplexer, and suitably selects and combines an image signal to be displayed on the display panel. Furthermore, at this time, the CPU 17106 generates a control signal to the display panel controller 17102 in accordance with the image signal to be displayed, and controls suitably an operation of the display device such as an image display frequency, a scanning method (for example, interlace or non-interlace), and the number of scanning lines on one screen.

[0159] Moreover, the CPU directly outputs image data and character/graphical information to the foregoing image generating circuit 17107, or accesses an external computer and a memory via the foregoing I/O inter-

face circuit 17105 to input the image data and the character/graphical information. Note that the CPU 17106 may be concerned with operations for other objects than these. For example, the CPU 17106 may concern directly a function to generate and process information as a personal computer and a word processor. Alternatively, as described above, the CPU 17106 is connected to the external computer network via the I/O interface circuit 17105, and may perform an operation such as a numerical calculation cooperatively with external equipment.

[0160] Moreover, the input section 17114 is for inputting an instruction, a program or data to the foregoing CPU 17106 by users, and it is possible to use various kinds of input equipment including as a joystick, a barcode reader and a voice recognition device in addition to a keyboard and a mouse.

[0161] Furthermore, the decoder 17104 is a circuit for inversely converting various kinds of image signals, which are input from the image generating signal 17107 and the TV signal receiving circuit 17113, to three primary color signals, luminance signals, I signals and Q signals. As shown by the dotted lines in Fig. 17, the decoder 17104 should provide an image memory. This is because the TV signals requiring the image memory in inversely converting are used in the MUSE method or like.

[0162] By providing the image memory, the display of the still image is made to be easier, or advantages that image processings such as thinning, an interpolation, a magnification, a reduction and a synthesis of an image can be performed easier by cooperating with the foregoing image generating circuit 17107 and the CPU 17106 are created.

[0163] Moreover, the multiplexer 17103 suitably selects the display image based on the control signal input from the foregoing CPU 17106. Specifically, the multiplexer 17103 selects a desired image signal among the image signals which were input from the decoder 17104 and were inversely converted, and outputs it to the driving circuit 17101. In this case, by switching and selecting the image signal within one screen display time, it is possible to divide one screen into a plurality of areas and display different images on the respective areas, like so called a multi-screen television.

[0164] The display panel controller 17102 is a circuit for controlling an operation of the driving circuit 17101 based on the control signal input from the foregoing CPU 17106.

[0165] With reference to a basic operation of the display panel, a signal for controlling an operation sequence of, for example, a driving power source (not shown) of the display panel is input to the driving circuit 17101. Moreover, with reference to a driving method of the display panel, a signal for controlling, for example, a screen display frequency and a scanning method (for example, interlace or non-interlace) is output to the driving circuit 17101.

[0166] A control signal concerning an adjustment of an image such as luminance, contrast, color tone and sharpness of the image is, in some cases, output to the driving circuit 17101.

[0167] Furthermore, the driving circuit 17101 is a circuit for generating the driving signal applied to the display panel 17100, and operates based on the image signal input from the foregoing multiplexer 17103 and the control signal input from the foregoing display panel controller 17102.

[0168] As above, the function of each portion was described. With the constitution exemplified in Fig. 17, it is possible to display the image information input from various kinds of image information source on the display panel 17100 in the present display device. Specifically, after various kinds of image signals in the television broadcast and like are inversely converted in the decoder 17104, the image signals inversely converted are suitably selected in the multiplexer 17103, and are input to the driving circuit 17101. On the other hand, the display controller 17102 generates the control signal for controlling an operation of the driving circuit 17101 in response to the image signal to be displayed. The driving circuit 17101 applies the driving signal to the display panel 17100 based on the foregoing image signal and the control signal. Thus, the image is displayed on the display panel 17100. A series of these operations are controlled overall by the CPU 17106.

[0169] The present display device displays the image selected from the image memory incorporated in the foregoing decoder 17104, the image generating circuit 17107, and information. In addition to this, the present display device can perform image processings including magnification, reduction, rotation, movement, edge emphasis, thinning, interpolation, color conversion, and image aspect ratio conversion, and image edition including synthesis, erasure, connection, replacement and insertion. In this em-

bodiment, though no description was made in the explanation of this embodiment, an exclusive-use circuit for performing a processing and an edition for voice information may be provided similarly to the foregoing image processing and the image edition.

[0170] Accordingly, the present display device can have functions of a display equipment of a television broadcast, a terminal equipment of a television conference, an image edition equipment for dealing with a still image and a moving picture, an terminal device of a computer, an office terminal equipment including a word processor, and a game machine by itself. The present display device shows a very wide application range in industrial use and in household use.

[0171] Fig. 17 merely shows an example of a constitution of the display device using a display panel in which an electron beam source is adopted as a surface conduction type electron emission device. As a matter of course, the constitution of the display device is not limited to this. For example, among the constituent components of Fig. 17, circuits relating to functions which are unnecessary in some applications may be omitted. Moreover, on the contrary, constituent components may be added depending on intended purposes. For example, in the case where the present display device is applied to a television telephone, it is preferable that a transmitter/receiver circuit including a television camera, a voice microphone, an illuminator and a modem is added to the constituent component.

[0172] In the present display device, since the display panel especially using the surface conduction type electron emission device as the electron beam can be easily made to be thin, it is possible to make the depth of the display device small. In addition, since the display panel using the surface conduction type electron emission device as the electron beam source can easily be made so as to have a large screen easily and shows high luminance and excellent field angle characteristic, the present display device can display an image abound in realistic sensations and stringency with a good visibility.

[0173] (Embodiment 4) This embodiment is an example of an image formation apparatus having many surface conduction type electron emission devices and the control electrode (gird).

[0174] A manufacturing method of the image formation apparatus of this embodiment was prepared by almost the same method as that of the em-

bodiment 2, and descriptions for it are made in detail.

[0175] First, made are descriptions for an electron source in which many surface conduction type electron emission devices are provided on a substrate and for an embodiment of a display device which applies the electron source. Fig. 19 and Fig. 20 are schematic views for explaining two examples of the electron source in which many surface conduction type electron emission devices are arranged.

[0176] First, in Fig. 19, reference symbol S denotes an insulating substrate using glass as its material, reference symbol ES surrounded by a dotted line denotes each of surface conduction type electron emission devices, and reference symbols E1 to E10 denote wiring electrodes for wiring the foregoing surface conduction type electron emission devices. The surface conduction type electron emission devices are formed in columns along the X-direction on the substrate (hereinafter referred to as device columns). The surface conduction type electron emission devices constituting the device columns are in common wired in parallel electrically by wiring electrodes of both sides sandwiching them. For example, the first column is wired by the wiring electrodes E1 and E2 on both sides thereof.

[0177] The electron source of this embodiment can drive the device columns independently from each other by applying a suitable driving voltage between the wiring electrodes. Specifically, a suitable voltage exceeding an electron emission threshold value should be applied to device columns desired to emit an electron beam, and a suitable voltage (for example, 0 [V]) below the electron emission threshold value should be applied to device columns emitting no electron beam. Note that in the below explanation, the suitable voltage exceeding the electron emission threshold value is referred to as VE [V].

[0178] Next, another example of the electron source is shown in Fig. 20. Reference symbol S denotes an insulating substrate using, for example, glass as its material, ES surrounded by a dotted line denotes a surface conduction type electron emission device provided on the substrate S and E'1 to E'6 denote wiring electrodes for wiring in common the foregoing surface conduction type electron emission devices. Similarly to the foregoing example of Fig. 19, also in this embodiment, the surface conduction type electron emission devices are formed in column along the X-direction, and

the surface conduction type electron emission device of the device columns are in common wired electrically in parallel by the wiring electrodes. Moreover, as the wiring electrode E'2 serves also as the common wirings of the first and second device columns on one side, one wiring electrode serves as the common electrode on the adjacent side of the device columns in this embodiment. The electron source of this embodiment has an advantage that an arrangement interval arranged in the Y-direction can be made to be small compared to the foregoing column of Fig. 19, in the case where the surface conduction type electron emission devices and the wiring electrodes, both having the same shape, are used.

[0179] The electron source of this embodiment can drive the device columns independently from each other, by applying a suitable driving voltage between the wiring electrodes. Specifically, VE [V] should be applied to electron emission device columns desired to emit electrons, and, for example, 0 [V] should be applied to device columns which are not allowed to emit electrons. For example, when only the third column is desired to be driven, a potential of 0 [V] is applied to the wiring electrodes of E'1 to E'3, and a potential of VE [V] is applied to the wiring electrodes of E'4 to E'6. As a result, a voltage equal to  $VE - 0 = VE$  [V] is applied to the third device column, and a voltage of 0 [V] including  $0 - 0 = 0$  [V] or  $VE - VE = 0$  [V] is applied to other device columns. Moreover, when the second and fifth columns are simultaneously driven, the potential of 0 [V] should be applied to the wiring electrodes E'1, E'2 and E'6, and the potential of VE [V] should be applied to the wiring electrodes E'3 and E'5. As described above, also in this embodiment, it is possible to drive selectively any device column.

[0180] In the electron source of Fig. 19 and Fig. 20, though the twelve surface conduction type electron emission devices are arranged per one column in the X-direction for convenience of illustration, the number of devices is not limited to this, and more surface conduction type electron emission devices may be arranged. Moreover, though the five device columns are arranged in the Y-direction, the number of device columns is not limited to this, and more device columns may be arranged.

[0181] Next, a flat plate type CRT using the foregoing electron source will be explained with examples.

[0182] Fig. 21 is a view showing a panel structure of the flat plate type CRT

comprising the foregoing electron source of Fig. 17. In Fig. 17, reference symbol VC denotes a vacuum container formed of glass, and reference symbol FP that is a part of the vacuum container shows a face plate on the display plane side. In an inner surface of the face plate FP, a transparent electrode using, for example, ITO as its material is formed, and, on the transparent electrode, red, green and blue phosphors are painted in mosaic shape or stripe shape. To prevent complexity of the drawing, a transparent electrode and the phosphors are denoted by reference symbol PH in Fig. 21. A known black matrix or a known black stripe may be provided between the phosphors, each having respectively red, green and blue color in the field of the CRT. Moreover, a known metal back layer can be also formed on each phosphor. The foregoing transparent electrode is electrically connected to the outside of the vacuum container via the terminal EV so that an accelerated voltage of the electron beam can be applied.

[0183] Moreover, reference symbol S denotes a substrate of an electron source fixed to the bottom of the vacuum container VC, and the surface conduction type electron emission device is formed on the substrate as described in Fig. 19. In this embodiment, the 200 device columns; having the 200 surface conduction type electron emission devices wired in parallel per a column, are provided. Two wiring electrodes of each device column are alternately connected to the electrode terminals Dp1 to Dp200 and Dm1 to Dm200 provided on the panel side plane on both sides, and designed so that a driving electric signal is applied from the outside of the vacuum container.

[0184] Stripe-shaped grid electrodes GR are provided between the substrate S and the face plate FP. The grid electrodes GR are provided by 200 independently so as to be perpendicular to the foregoing device columns (specifically, in the Y-direction), and an opening Gh is provided in each grid electrode GR so as to allow the electron beam to pass therethrough. Each opening Gh is a circular shape and corresponds to corresponding one of the surface conduction type electron emission devices. In some cases, many mesh-shaped openings are provided. Each grid electrode is connected to the outside of the vacuum container electrically by the electrode terminals G1 to G200. The grid electrode is not always needed to have the shape and be disposed as shown in Fig. 21, as long as the grid electrode can modulate

the electron beam emitted from the surface conduction type electron emission device, and the grid electrode may be provided, for example, around the surface conduction type electron emission device or in the vicinity of it.

[0185] In the present display panel, the device columns of the surface conduction type electron emission devices and the grid electrodes compose  $200 \times 200$  XY matrix. Accordingly, by applying a modulating signal for one line of an image to the grid electrode column in synchronization with driving (scanning) the device column sequentially one by one, irradiation of each electron beam to the phosphor is controlled and an image is displayed one line by one line.

[0186] Next, Fig. 22 is a block diagram of an electric circuit for driving the foregoing display panel of Fig. 21. In Fig. 22, reference numeral 1000 denoted the display panel of Fig. 21; 1001, a decode circuit for decoding a complex image signal input from the outside; 1002, a serial/parallel conversion circuit; 1003, a line memory; 1004, a modulation signal generating circuit; 1005, a timing control circuit; and 1006, a scanning signal generating circuit. Electrode terminals of the display panel 1000 are connected to the electrical circuit, and the terminal EV is connected to a voltage source HV for generating an acceleration voltage of 10 [kV], and terminals G1 to G20 are connected to the modulation signal generating circuit 1004. Terminals Dp1 to Dp200 are connected to the scanning signal generating circuit 1006, and terminals Dm1 to Dm200 are connected to the ground.

[0187] Functions of each portion will be described below. First, the decode circuit 1001 is a circuit for decoding the complex image signal such as a NTSC television signal input from the outside, and separates a luminance signal component and a synchronous signal component from the complex image signal. The decode circuit 1001 outputs the former to the serial/parallel conversion circuit 1002 as a Data signal, and the latter to the timing control circuit 1005 as a Tsync signal. Specifically, the decode circuit 1001 arranges luminance for each color component RGB so as to match the color image arrangement of the display panel 1000, and output sequentially to the serial/parallel conversion circuit 1002. Moreover, the decode circuit 1001 extracts a vertical synchronization signal and a horizontal synchronization signal and outputs them to the timing control circuit 1005. The timing control circuit 1005 generates various kinds of timing control

signals for matching an operation timing of each portion with others, based on the foregoing synchronous signal  $T_{sync}$ . In other words, the timing control circuit 1005 outputs  $T_{sp}$  to the serial/parallel conversion circuit 1002,  $T_{mry}$  to the line memory 1003,  $T_{mod}$  to the modulation signal generating circuit 1004, and  $T_{scan}$  to the scanning signal generating circuit 1006.

[0188] The serial/parallel conversion circuit 1002 sequentially samples the luminance signal  $Data$  input from the decode circuit 1001 based on the timing signal  $T_{sp}$  input from the timing control circuit 1005, and outputs them as 200 parallel signals  $I1$  to  $I200$  to the line memory 1003. The timing control circuit 1005 outputs the writing timing control signal  $T_{mry}$  to the line memory 1003 when data for one line of the image is serially/parallelly converted. Upon receipt of the timing control signal  $T_{mry}$ , the line memory 1003 stores contents of the parallel signals  $I1$  to  $I200$ , and outputs them as  $I'1$  to  $I'200$  to the modulation signal generating circuit 1004. This is stored until a subsequent writing timing control signal  $T_{mry}$  is input to the line memory.

[0189] The modulation signal generating circuit 1004 is a circuit for generating a modulation signal to be applied to the grid electrode of the display panel 1000, based on luminance data for one image line input from the line memory 1003, and simultaneously applies the modulation signal to the modulation signal terminals  $G1$  to  $G200$  in synchronization with the timing control signal  $T_{mod}$  generated by the timing control circuit 1005. A voltage modulation method in which the modulation signal changes a level of the voltage in accordance with luminance data is used, and a pulse width modulation method in which a length of a voltage pulse is changed in accordance with the luminance data may be used.

[0190] Moreover, the scanning signal generating circuit 1006 is a circuit for generating voltage pulses for suitably driving the device columns of the surface conduction type electron emission devices of the display panel 1000. The scanning signal generating circuit 1006 suitably switches switching circuits therein in accordance with the timing control signal  $T_{scan}$  generated by the timing control circuit 1005, and applies to the terminals  $Dp1$  to  $Dp200$  selectively either a suitable driving voltage  $VE$  [V] exceeding the threshold value of the surface conduction type electron emission device, emitted by a constant voltage source  $DV$ , or a ground level (specifically, 0

[V]).

[0191] By the above described circuits, drive signals are applied to the display panel 1000 at a timing shown in the timing chart of Fig. 23. Figs. 23(a) to 23(d) show a part of signals applied to the terminals Dp1 to Dp200 of the display panel from the scanning signal generating circuit 1006, and, as understood from the drawings, a voltage pulse of an amplitude  $VE$  [E] is sequentially applied to the terminals Dp1, Dp2, Dp3,...at every one line display time. On the other hand, since the terminals Dm1 to Dm100 are always connected to the ground level (0 [V]), the device columns are sequentially driven by the foregoing voltage pulses from the first columns, and an electron beam is sequentially output.

[0192] Moreover, a modulation signal for one line of an image is simultaneously applied to the terminals G1 to G200 from the modulation signal generating circuit 1004 at timings shown in Fig. 23(f) in dotted lines in synchronization with this. Also the modulation signal is sequentially switched in synchronization with switching the scanning signal, and an image for one screen is sequentially displayed. By repeating this continuously, a television moving picture can be displayed.

[0193] Hitherto, the flat plate type CRT comprising the electron source of Fig. 19 was described. Next, a flat plate type CRT comprising the foregoing electron source of Fig. 20 will be explained using Fig. 22.

[0194] The flat plate type CRT of Fig. 24 has a structure that the electron source of the flat plate type CRT of Fig. 21 is replaced with a type of Fig. 20. A  $200 \times 200$  XY matrix is constituted by the electron emission device columns and the grid electrodes. Since the surface conduction type electron emission devices of 200 columns are wired by the 201 wiring electrodes E1 to E201, the 201 electrode terminals Ex1 to Ex201 are provided in the vacuum container.

[0195] A driving circuit for driving the display panel 1008 is shown in Fig. 25, and the driving circuit is principally the same as the circuit of G4 other than scanning signal generating circuit 1007. The scanning signal generating circuit 1007 outputs selectively either a suitable driving voltage  $VE$  [V] exceeding the electron emission threshold value of the surface conduction type electron emission device, generated by the constant voltage source DV, or the ground level (0 [V]) to the terminals of the display panel, and its

timing is shown in the timing chart of Fig. 24. The display panel performs a display operation at timings shown in (a), and hence the driving signals shown in (b) to (e) are applied from the scanning signal generating circuit 1007 to the electrode terminals Ex1 to Ex4. Accordingly, the voltages shown in (f) to (h) are applied to the surface conduction type electron emission device columns, and the columns are sequentially driven one by one. In synchronization with this, the modulation signal is output from the modulation signal generating circuit 1004 at a timing shown in (i), and the image is displayed sequentially.

[0196] Also the image formation apparatus of this embodiment has the same effects as those of the embodiment 2.

[0197]

[Effects of the Invention] As described above, according to the present invention, by the activation treatment step of the electron emission device, a part of the electron emission portion is controllably covered with graphite, amorphous carbon or the covering film containing compound formed of them as a major constituent, so that the electron emission characteristic that has been unclear in vacuum can be controlled.

[0198] The activation treatment should include a step for covering a thin film containing carbon as a main constituent therein, and a step for applying a voltage equal to a voltage control type negative resistance characteristic region or more to a pair of electrodes of the electron emission device in vacuum, and the thin film containing carbon as a major constituent covers a area ranging from a part of the electron emission portion to the high potential side. Thus, the characteristic is more stable than that of the initial stage of driving of the electron emission device. The device current is small, and the high efficiency electron emission device can be prepared.

[0199] Moreover, the electron source emitting electrons in accordance with the input signal can be prepared stably and with a high yield. With an increase of efficiency, the cheap apparatus which consumes less power and reduces burden of the peripheral circuits can be provided.

[0200] In the image formation apparatus, the electron emission characteristic is stable and controllable and the efficiency is improved. For example, in the image formation apparatus using the phosphor as the image formation member, the image formation apparatus showing high luminance with

a low current and a high quality, for example, a color television, can be realized.

[Brief Description of the Drawings]

[Figure 1] Fig. 1 is a view showing a basic surface conduction type electron emission device according to the present invention.

[Figure 2] Fig. 2 is a view for explaining a basic manufacturing method of the surface conduction type electron emission device according to the present invention.

[Figure 3] Fig. 3 is a view of a measurement evaluation used for a characteristic evaluation of the surface conduction type electron emission device according to the present invention.

[Figure 4] Fig. 4 is a view showing an example of a voltage waveform in a forming treatment according to the present invention.

[Figure 5] Fig. 5 is a view showing a dependency of a device current and an emitted current of the surface conduction type electron emission device according to the present invention on an activation treatment time.

[Figure 6] Fig. 6 is a view showing a state change of the surface conduction type electron emission device according to the present invention by the activation treatment.

[Figure 7] Fig. 7 is a view showing a typical example of a relation among an emitted current, a device current and a device voltage of the surface conduction type electron emission device according to the present invention.

[Figure 8] Fig. 8 is a view showing a constitution of an electron source substrate according to the present invention.

[Figure 9] Fig. 9 is a view showing a basic constitution of an image formation apparatus according to the present invention.

[Figure 10] Fig. 10 is a view showing a phosphor film used in the image formation apparatus in Fig. 10.

[Figure 11] Fig. 11 is a view showing a surface conduction type electron emission device of an embodiment 1 of the present invention.

[Figure 12] Fig. 12 is a view showing a constitution of another embodiment of the basic surface conduction type electron emission device according to the present invention.

[Figure 13] Fig. 13 is a view partially showing a constitution of an electron source of an embodiment 2 according to the present invention.

[Figure 14] Fig. 14 is a section view taken along the line A-A' of Fig. 13.

[Figure 15] Fig. 15 is a section view for explaining a manufacturing steps of the electron source of the embodiment 2 according to the present invention.

[Figure 16] Fig. 16 is a section view for explaining a manufacturing steps of the electron source of the embodiment 2 according to the present invention.

[Figure 17] Fig. 17 is section views for explaining a display device of an embodiment 3 of the present invention.

[Figure 18] Fig. 18 is a view showing a constitution of a conventional surface conduction type electron emission device.

[Figure 19] Fig. 19 is a schematic constitutional view of an electron source substrate of an image formation apparatus of an embodiment 4 according to the present invention.

[Figure 20] Fig. 20 is a schematic constitutional view of an electron source substrate of an image formation apparatus of the embodiment 4 according to the present invention.

[Figure 21] Fig. 21 is a panel constitution view in the image formation apparatus of the embodiment 4 according to the present invention.

[Figure 22] Fig. 22 is a block diagram for explaining an electric circuit for driving the image formation apparatus of the embodiment 4 according to the present invention.

[Figure 23] Fig. 23 is a timing chart for explaining a drive of the image formation apparatus of the embodiment 4 according to the present invention.

[Figure 24] Fig. 24 is a panel constitution view in the image formation apparatus of the embodiment 4 according to the present invention.

[Figure 25] Fig. 25 is a block diagram for explaining an electric circuit for driving the image formation apparatus of the embodiment 4 according to the present invention.

[Figure 26] Fig. 26 is a timing chart for explaining a drive of the image formation apparatus of the embodiment 4 according to the present invention.

[Explanations of Reference Numerals]

1...substrate, 2...thin film for forming electron emission portion, 3...electron emission portion, 4...thin film including electron emission portion, 5 and 6...device electrode, 84 and 74...electron emission device, 82 and 83...wiring, 85...connection line, 91...rear plate, 92...supporting frame, 93...transparent substrate, 94...phosphor film, 95...metal back, 96...face

plate, 98...eneveloper, 141...interlayer insulating layer, and 142...contact hole.

Continued from the front page

(72) Inventor: Yoshikazu Sakano

CANON INC.

30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo

Fig. 1

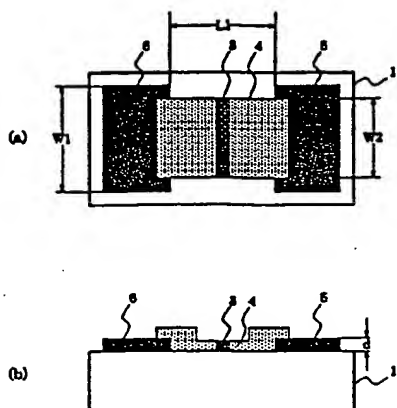


Fig. 2

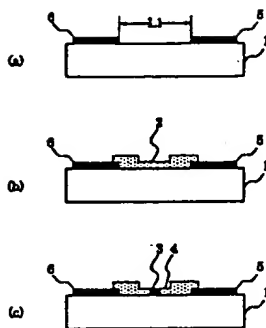


Fig. 4

Fig. 3

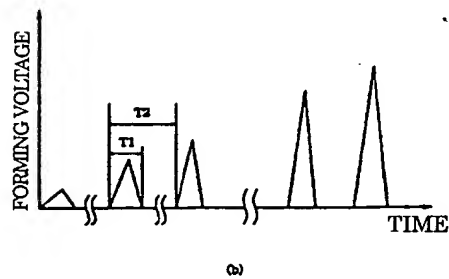
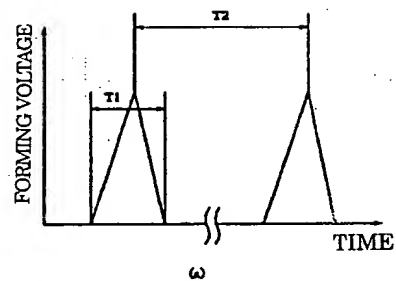
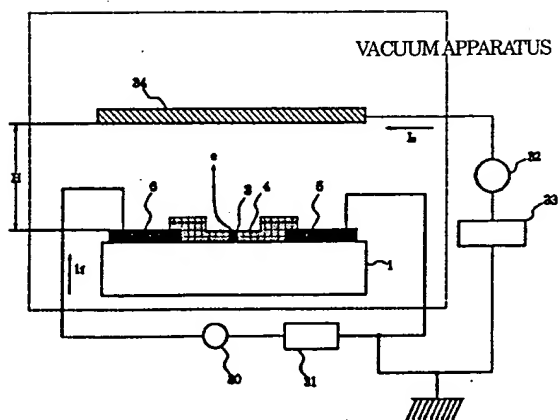


Fig. 5

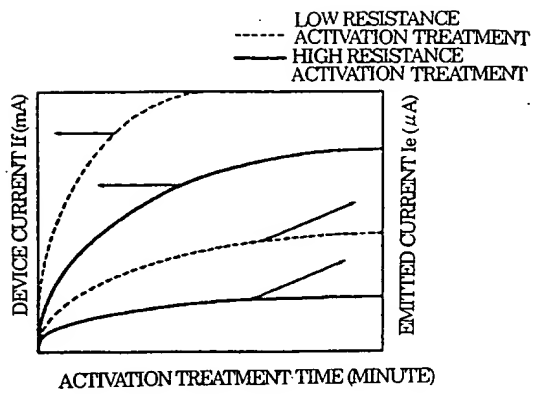


Fig. 6

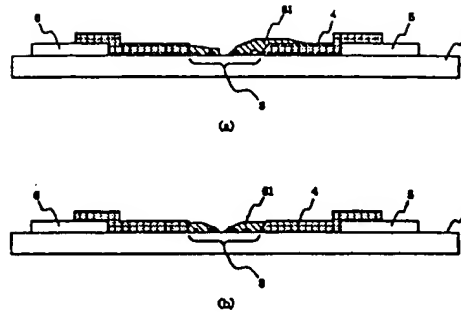


Fig. 7

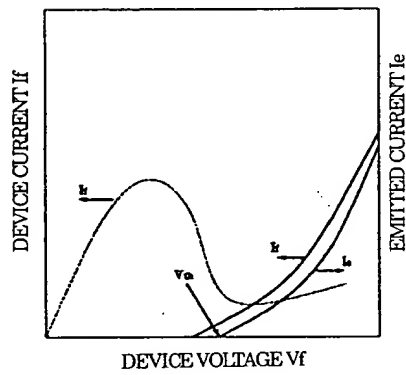


Fig. 8

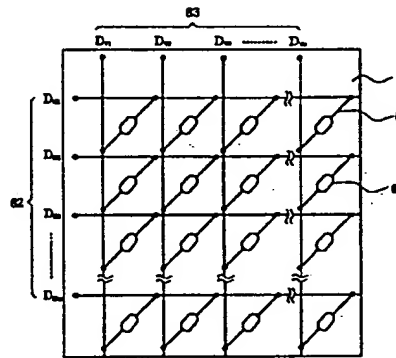


Fig. 9

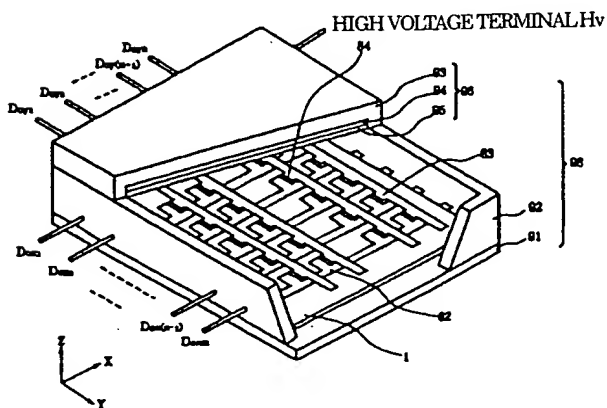


Fig. 11

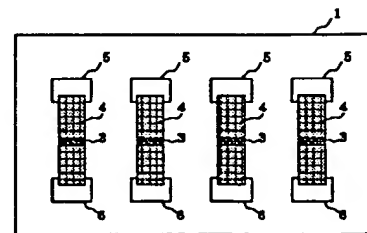


Fig. 12

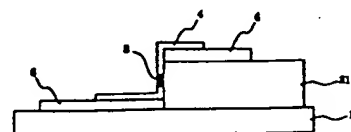


Fig. 10

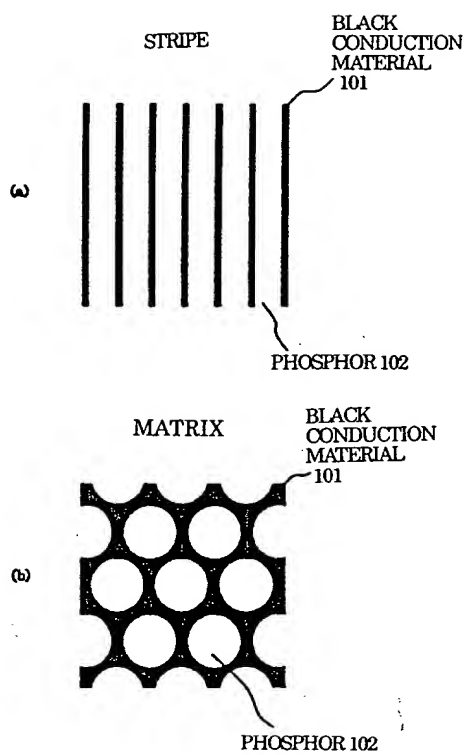


Fig. 13

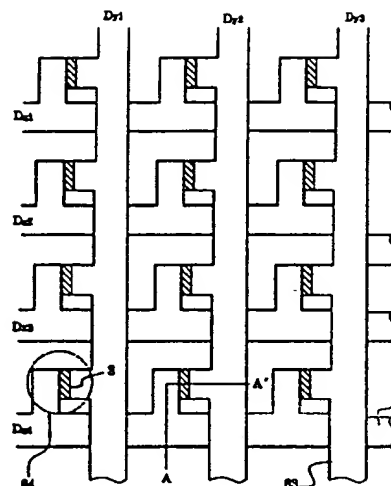


Fig. 15

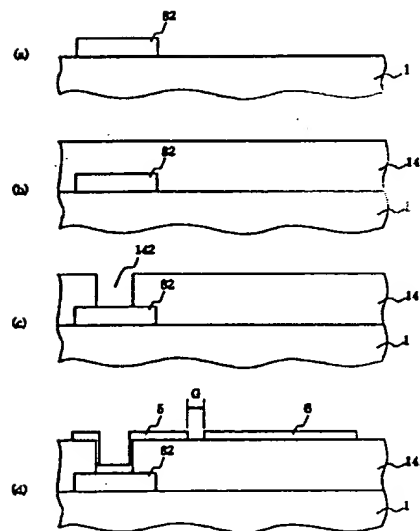


Fig. 14

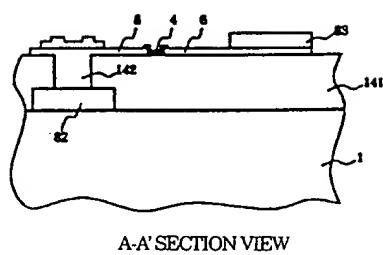


Fig. 16

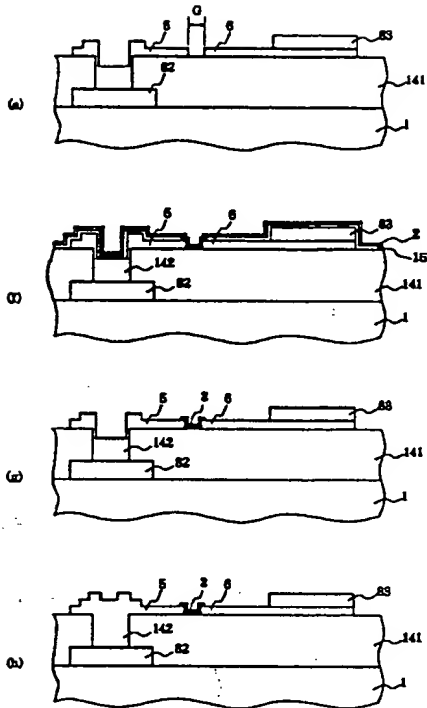


Fig. 18

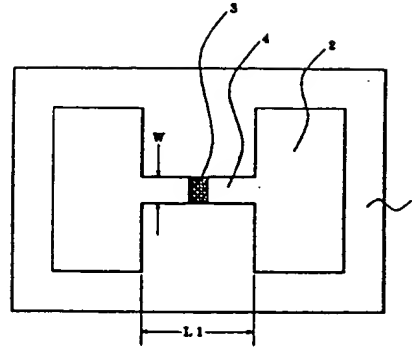


Fig. 20

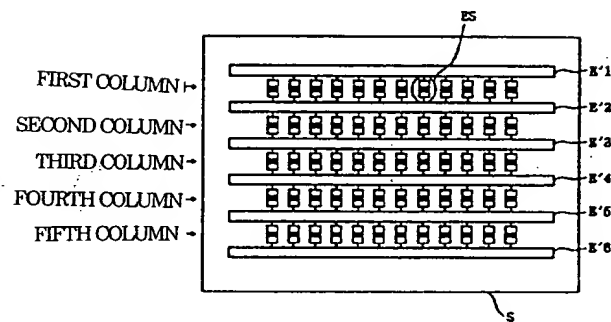


Fig. 19

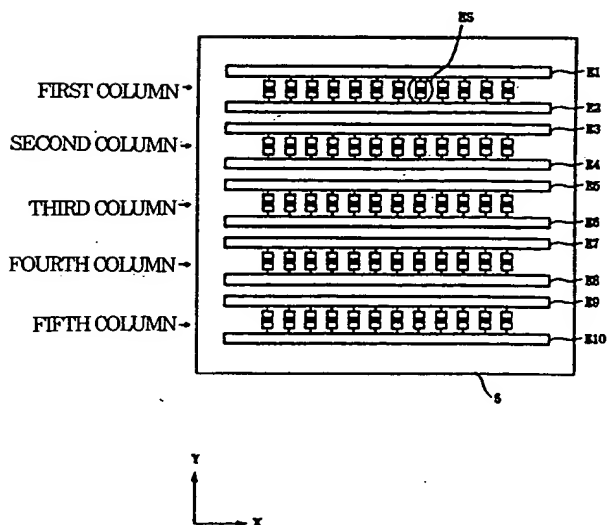


Fig. 17

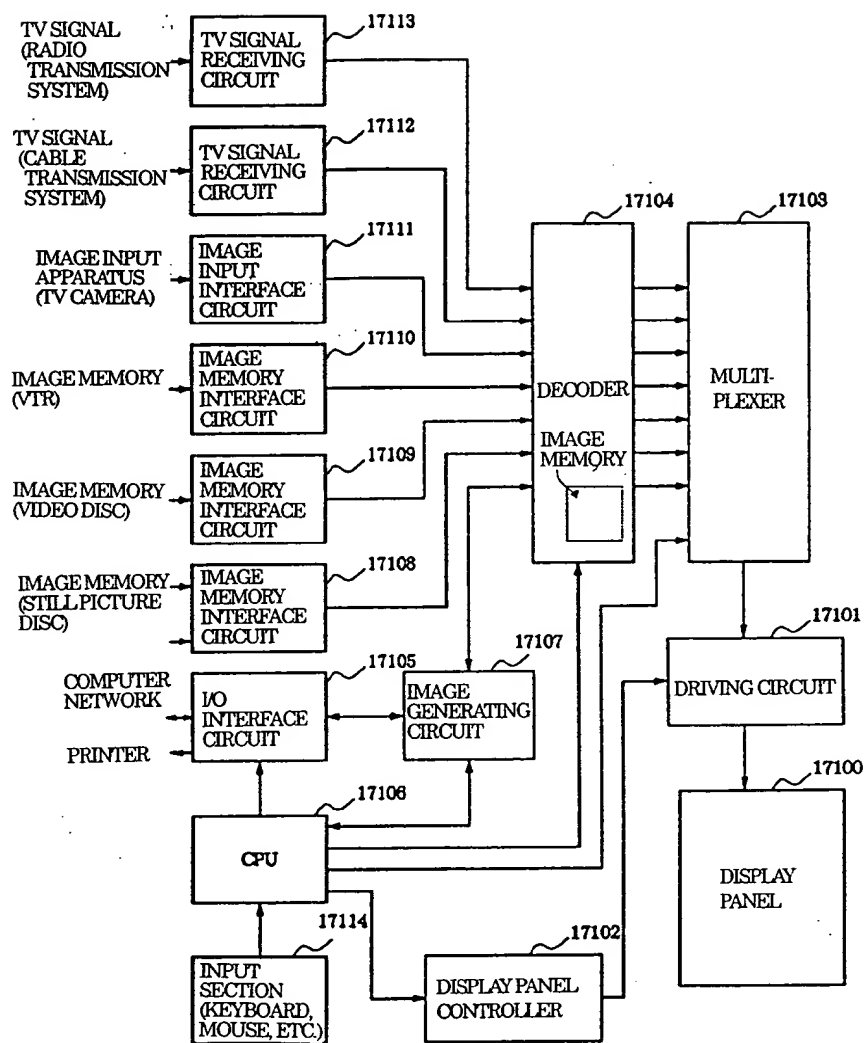


Fig. 21

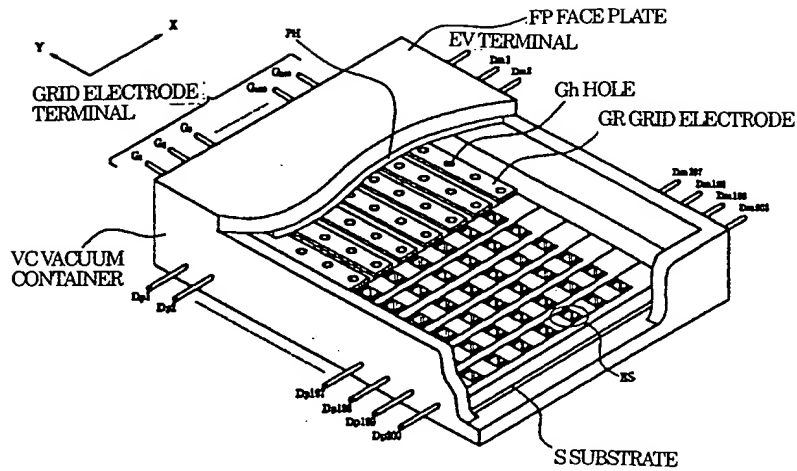


Fig. 22

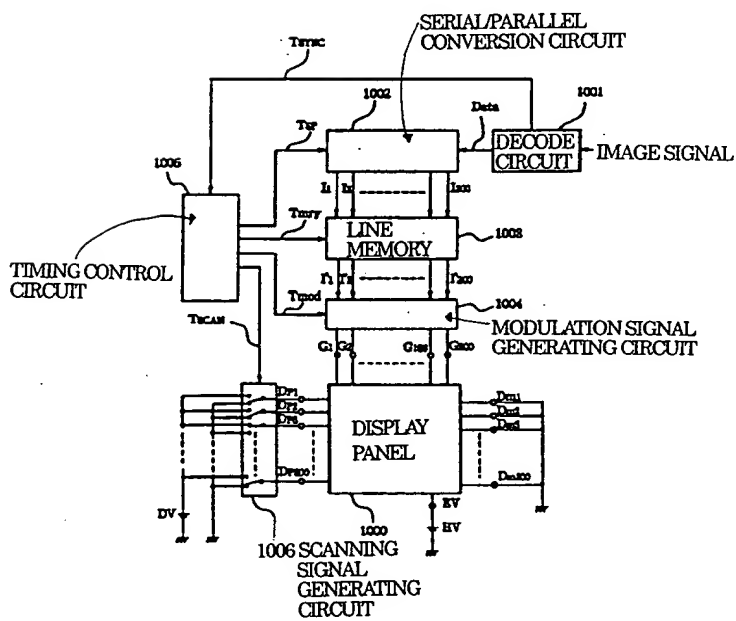


Fig. 23

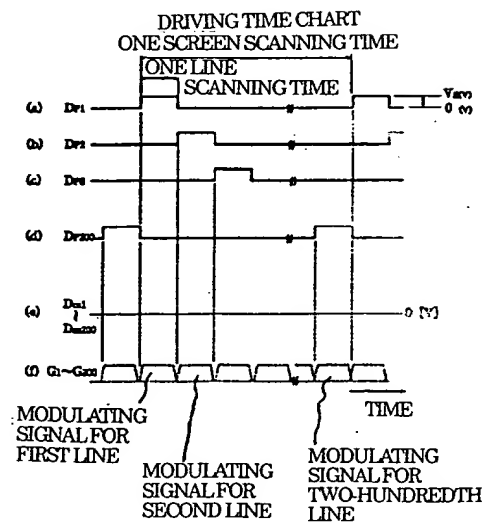


Fig. 24

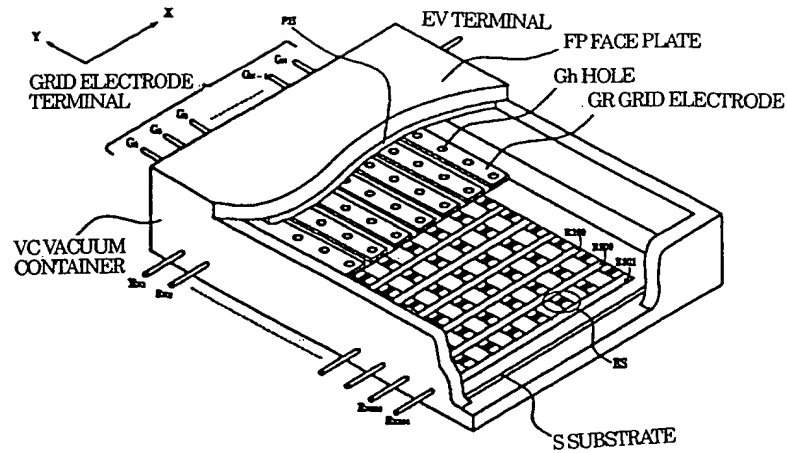


Fig. 25

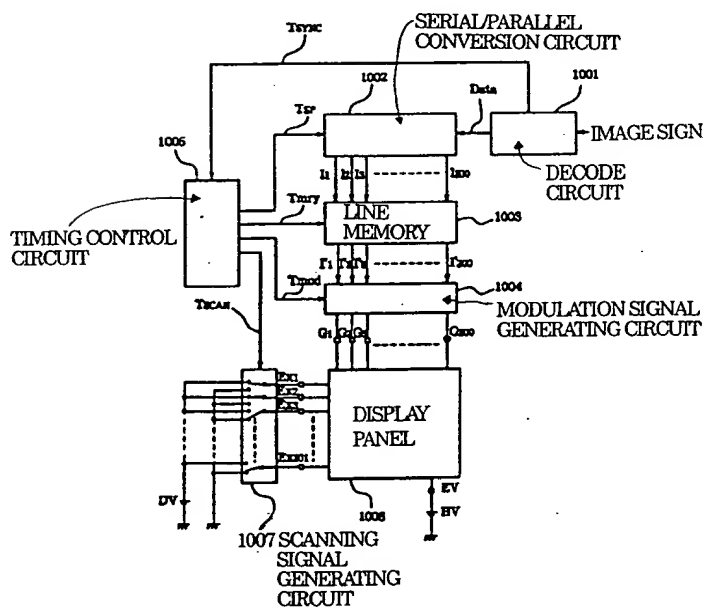


Fig. 26

